

Today

Analog ⇔ Digital Conversion

- **Sampled Data Acquisition Systems**
- **Discrete Sampling and Nyquist**
- **Digital to Analog Conversion**
- **Analog to Digital Conversion**

Analog → Digital → Analog

Benefits of digital systems

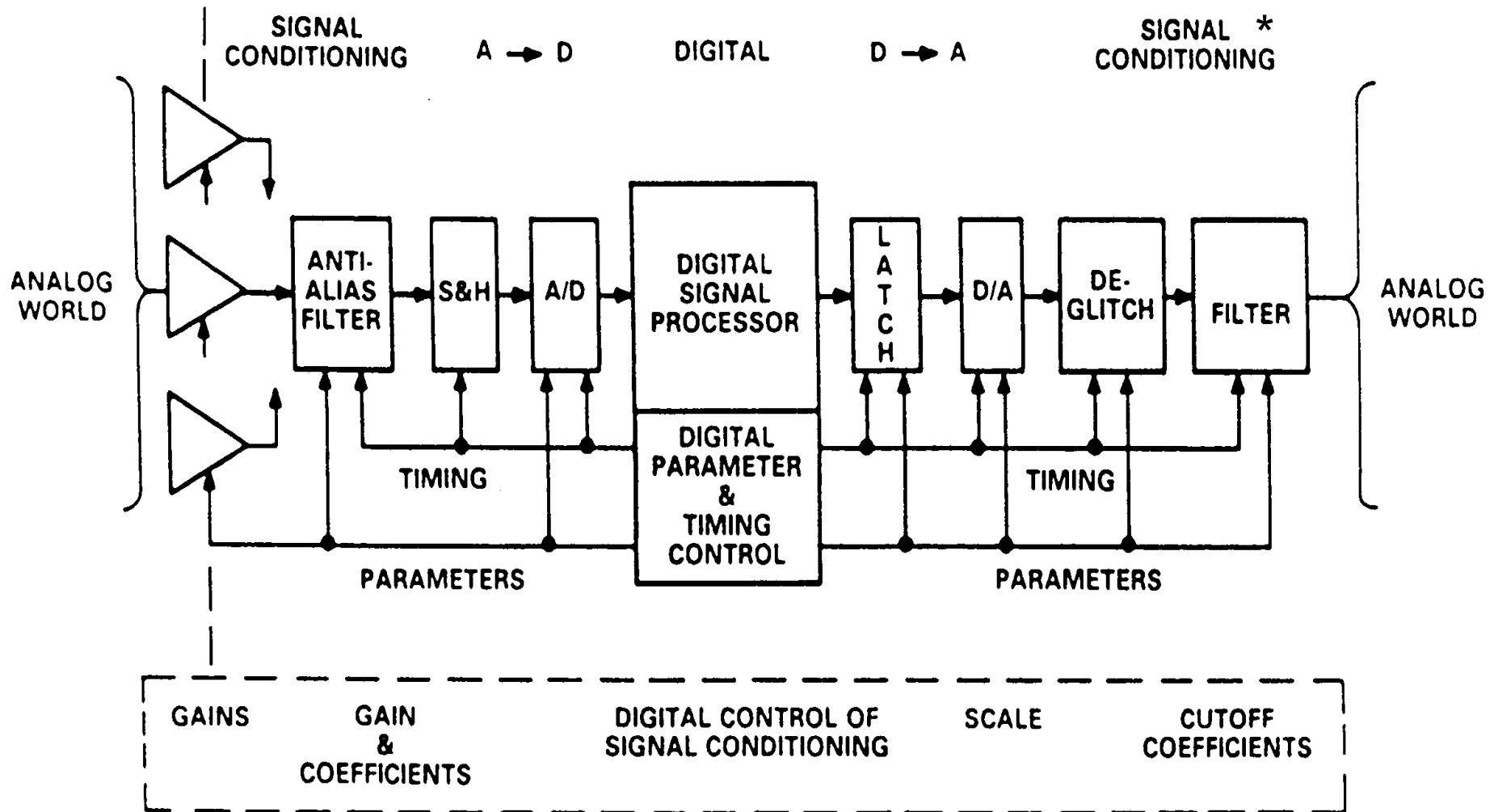
Digital signals “Immune” to noise

- Analog signal can lose accuracy due to noise added to the desired signal
- Digital, if no bits are lost, guarantees 100% accuracy
- Improved storage density
- More powerful signal processing

But,

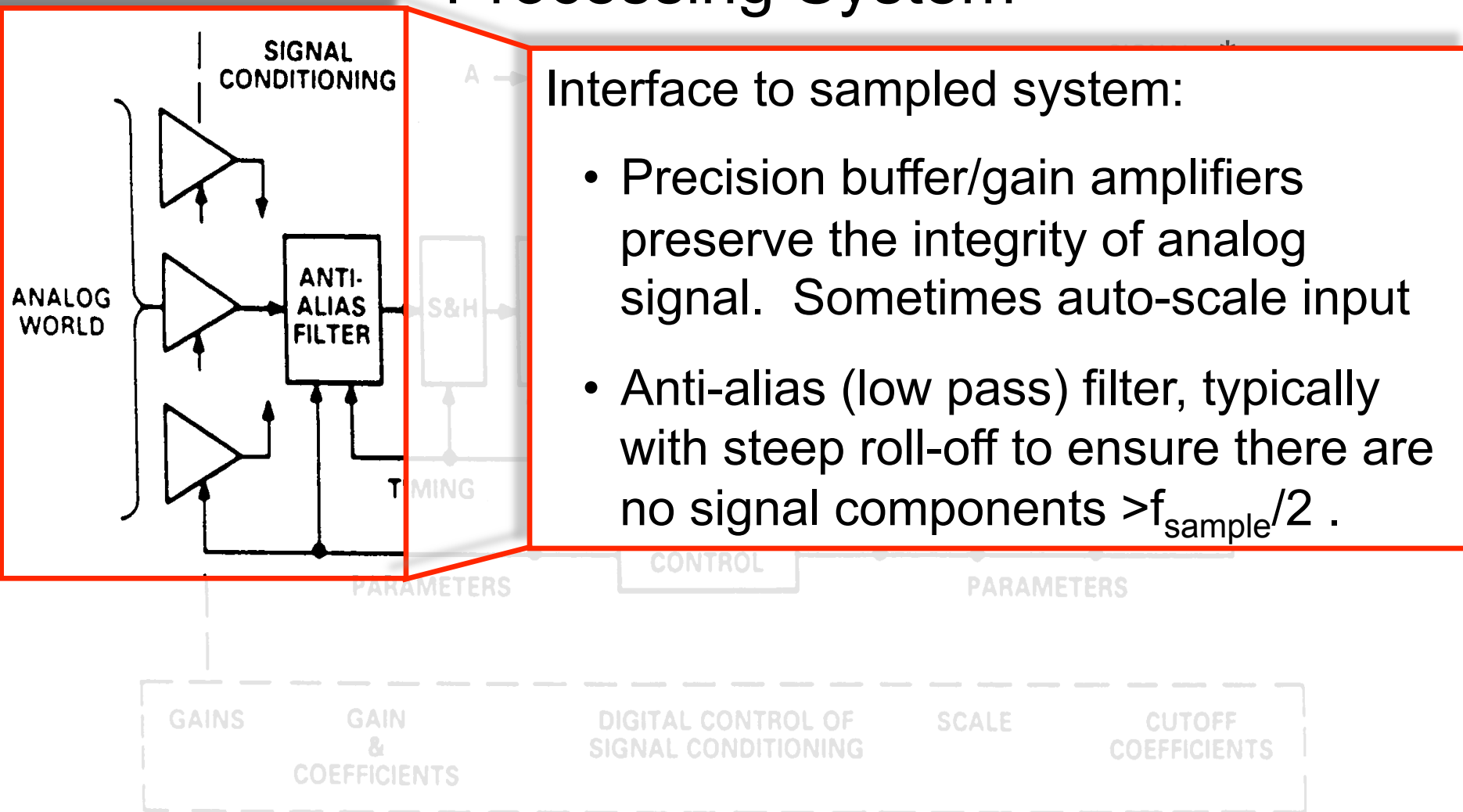
- Digital system is only precise up to least significant bit
- Getting analog to digital is not noiseless
- Digital systems also introduce high frequency “noise”

Key Elements of a Sampled Signal Processing System



An audio CD process would be an example of a system that has all of these components. (The recording artist is on the left ("Analog World"), the listener would be on the right. Some systems do not have all of these parts (e.g. a digital oscilloscope generally has no analog output.)

Key Elements of a Sampled Signal Processing System

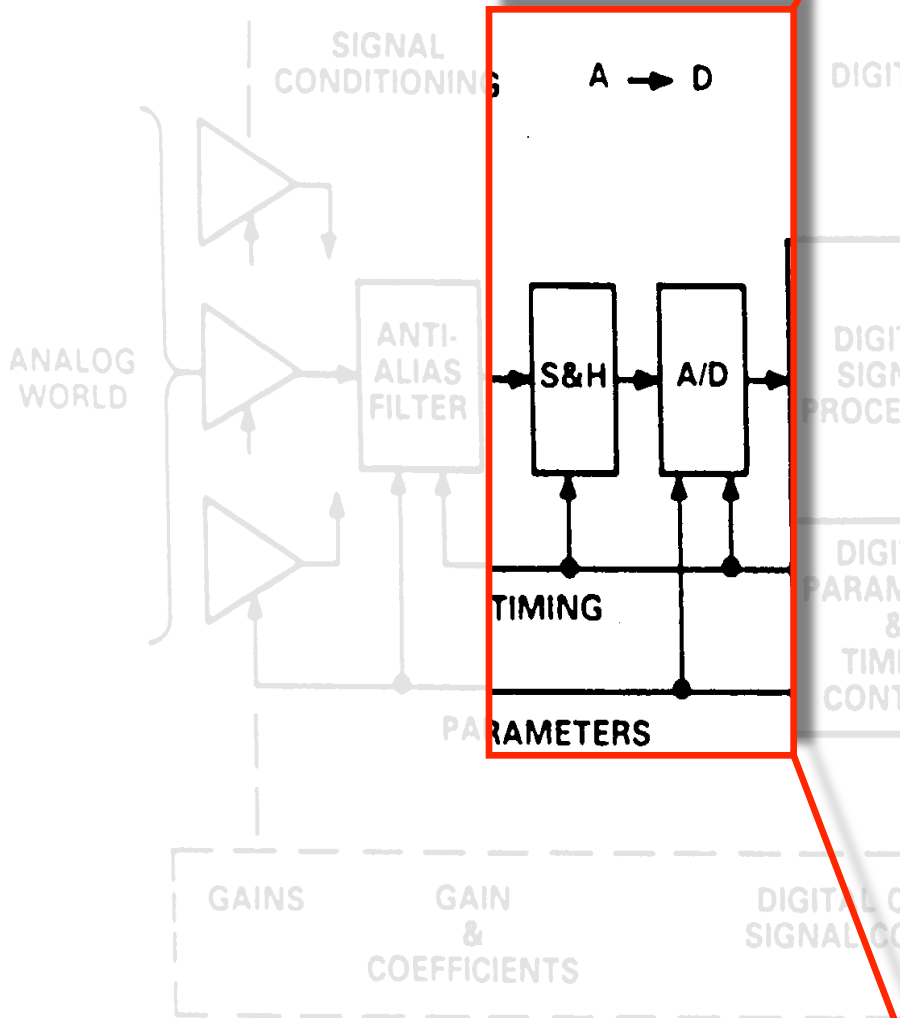


Interface to sampled system:

- Precision buffer/gain amplifiers preserve the integrity of analog signal. Sometimes auto-scale input
- Anti-alias (low pass) filter, typically with steep roll-off to ensure there are no signal components $> f_{\text{sample}}/2$.

*ref: Analog Devices; Application Note AN-282

Key Elements of Processing

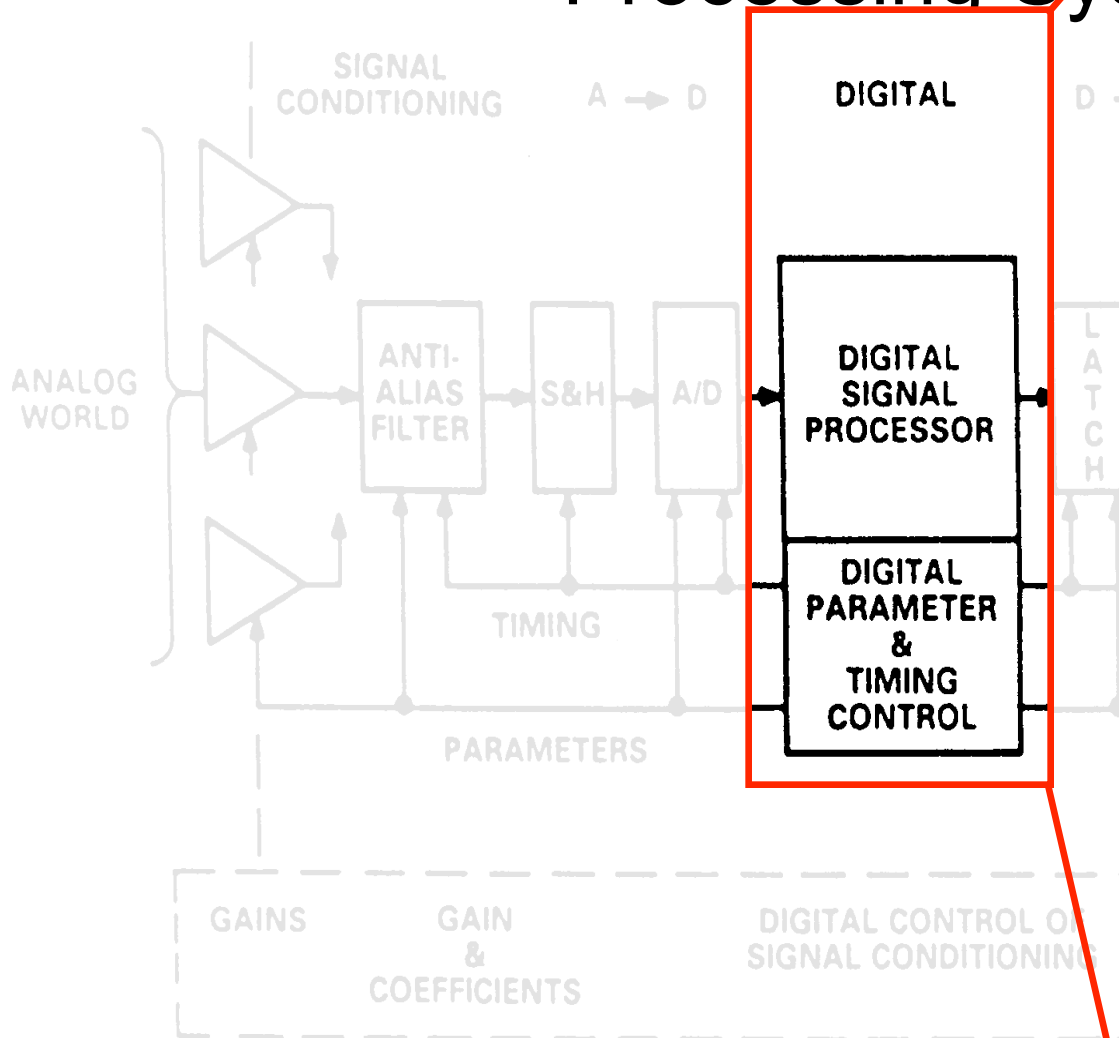


Converts the analog signal into a digital representation:

- Sample and Hold is analog circuitry that ensures the ADC sees a stable, unchanging signal for the time required to accurately perform the conversion. (allows for under-sampling – advanced topic in A/D)
- A/D can be any of a wide range of devices. More on this later.

*ref: Analog Devices; Application Note AN-282

Key Elements of a Sampled Signal Processing System



A *Digital Signal Processor (DSP)* is a microprocessor optimized for manipulating digitized analog signals:

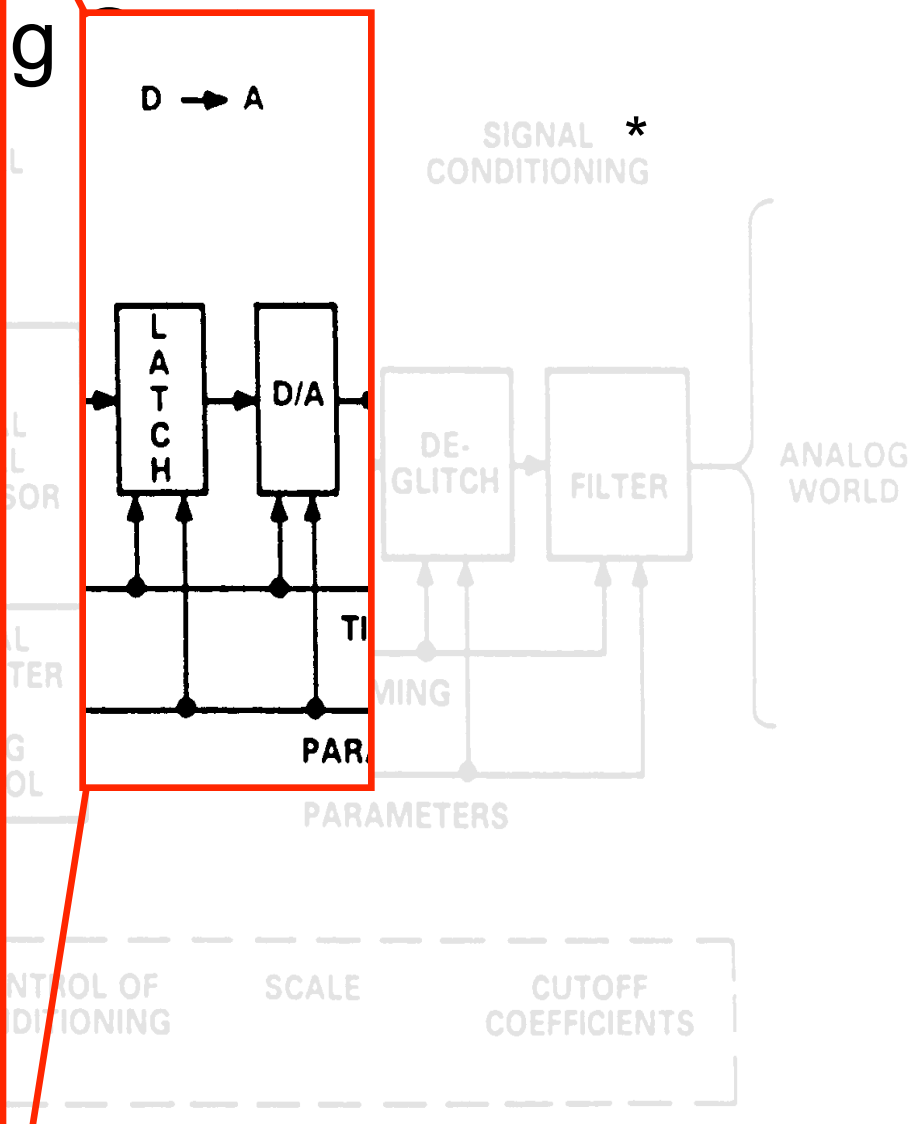
- Perform operations such as digital filtering and FFTs.
- Often is also used for system control.
- Vector processors. Field programmable gate arrays (FPGA).

*ref: Analog D

In many systems the signal is converted back into analog (sometimes after short or long term storage in memory):

- Latch holds the digital data until the D/A can finish the conversion. This also allows the DSP processor to move on to other tasks.
- The D/A reverses the process used on the input side of the system.
- Some systems are made to faithfully reproduce (CD players) or improve (noise cancelling headphones) on the original analog input.

a Sampled Signal

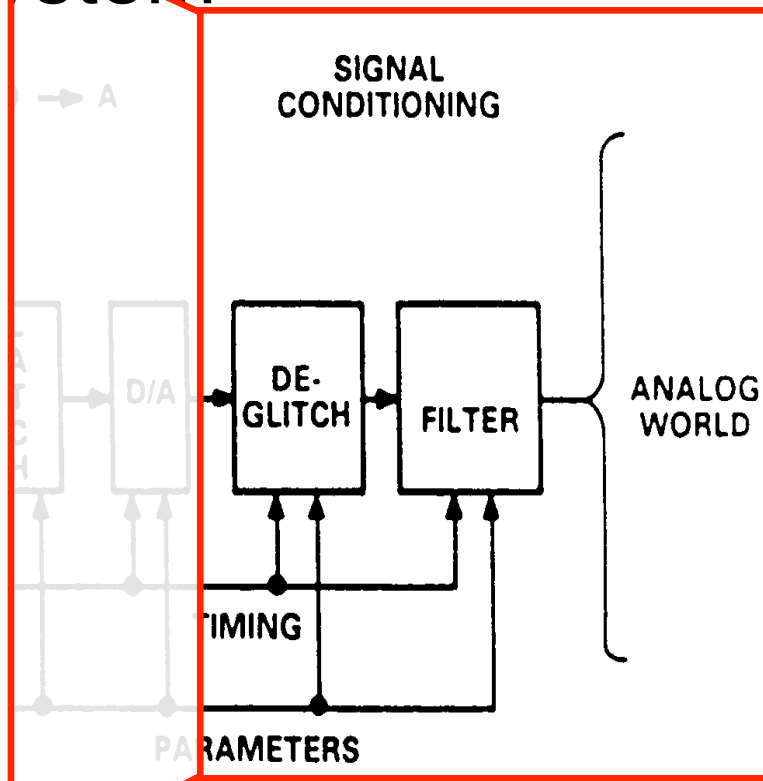


Key Elements of a Sampled Signal System

The final part of the process includes additional conditioning in the analog domain.

- Some D/As can produce in-band glitches that must be removed at this stage.
- Analog filtering can be used to compensate for the discrete nature of the D/A, improving overall system fidelity.

System



GAINS

GAIN
&
COEFFICIENTS

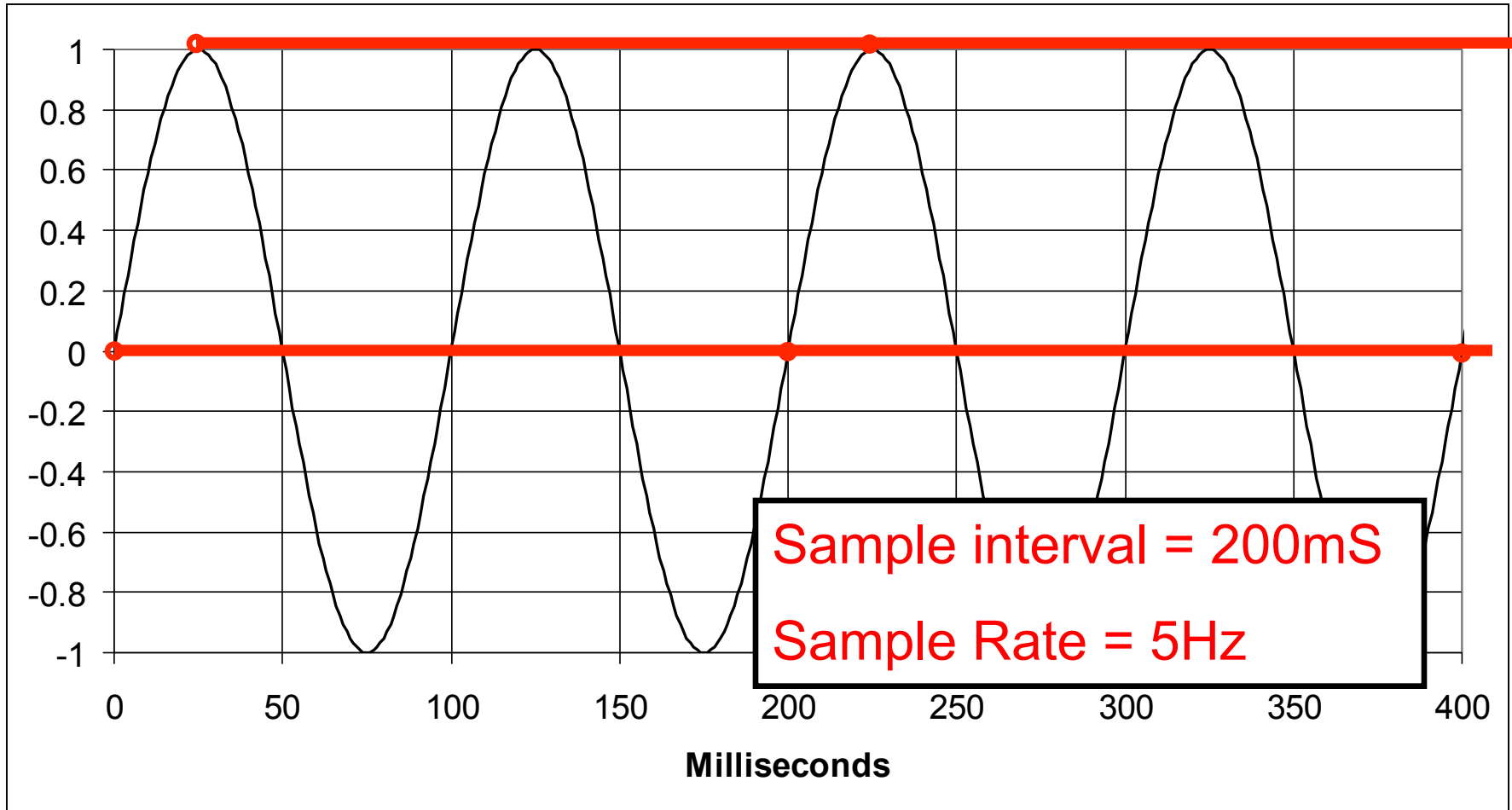
DIGITAL CONTROL OF
SIGNAL CONDITIONING

SCALE

CUTOFF
COEFFICIENTS

*ref: Analog Devices; Application Note AN-282

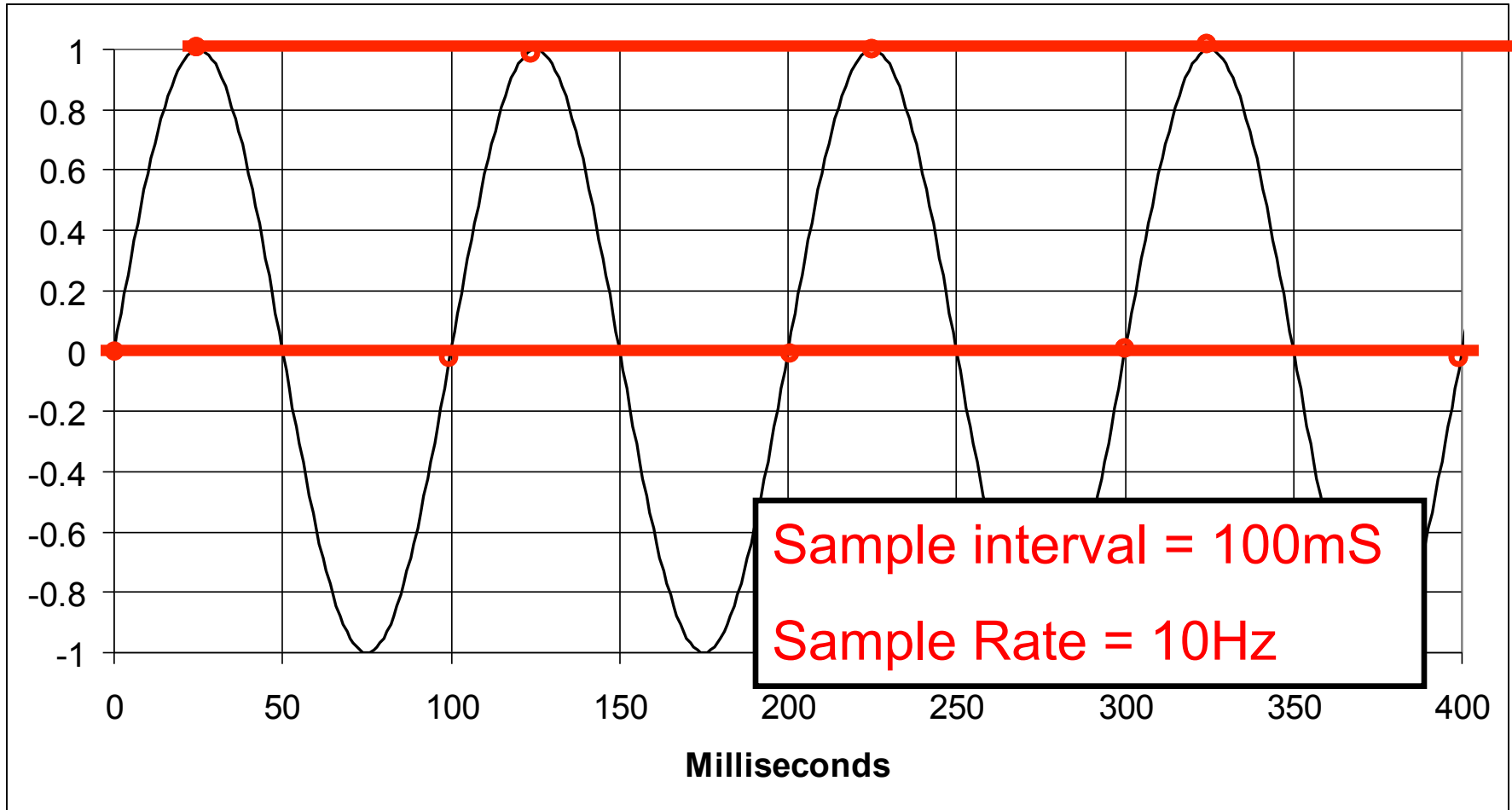
Discrete Sampling at 5Hz



$$f_F = 10Hz$$

$$f_S = 5Hz$$

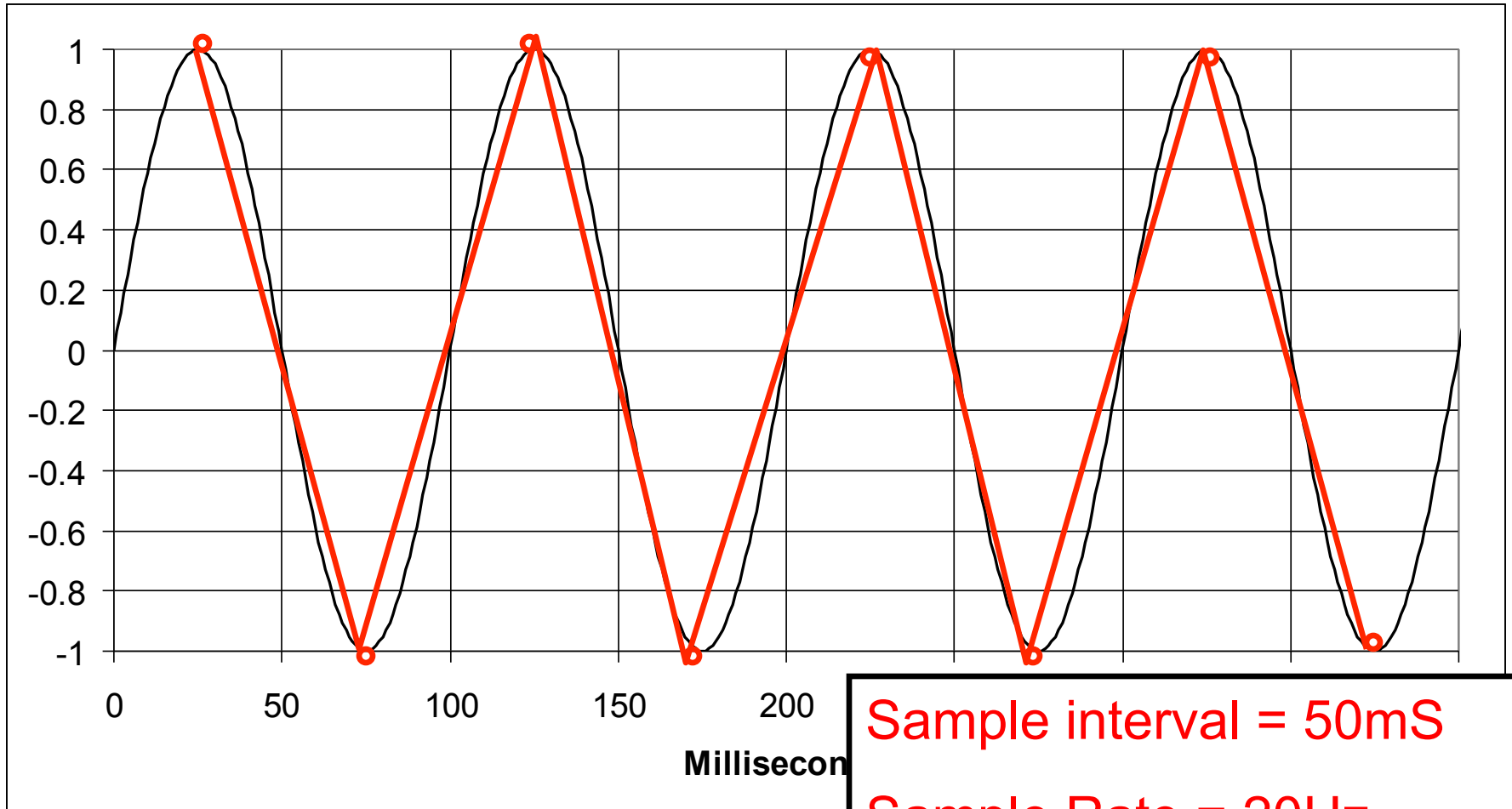
Discrete Sampling at 10Hz



$$f_F = 10Hz$$

$$f_S = 10Hz$$

Discrete Sampling at 20Hz

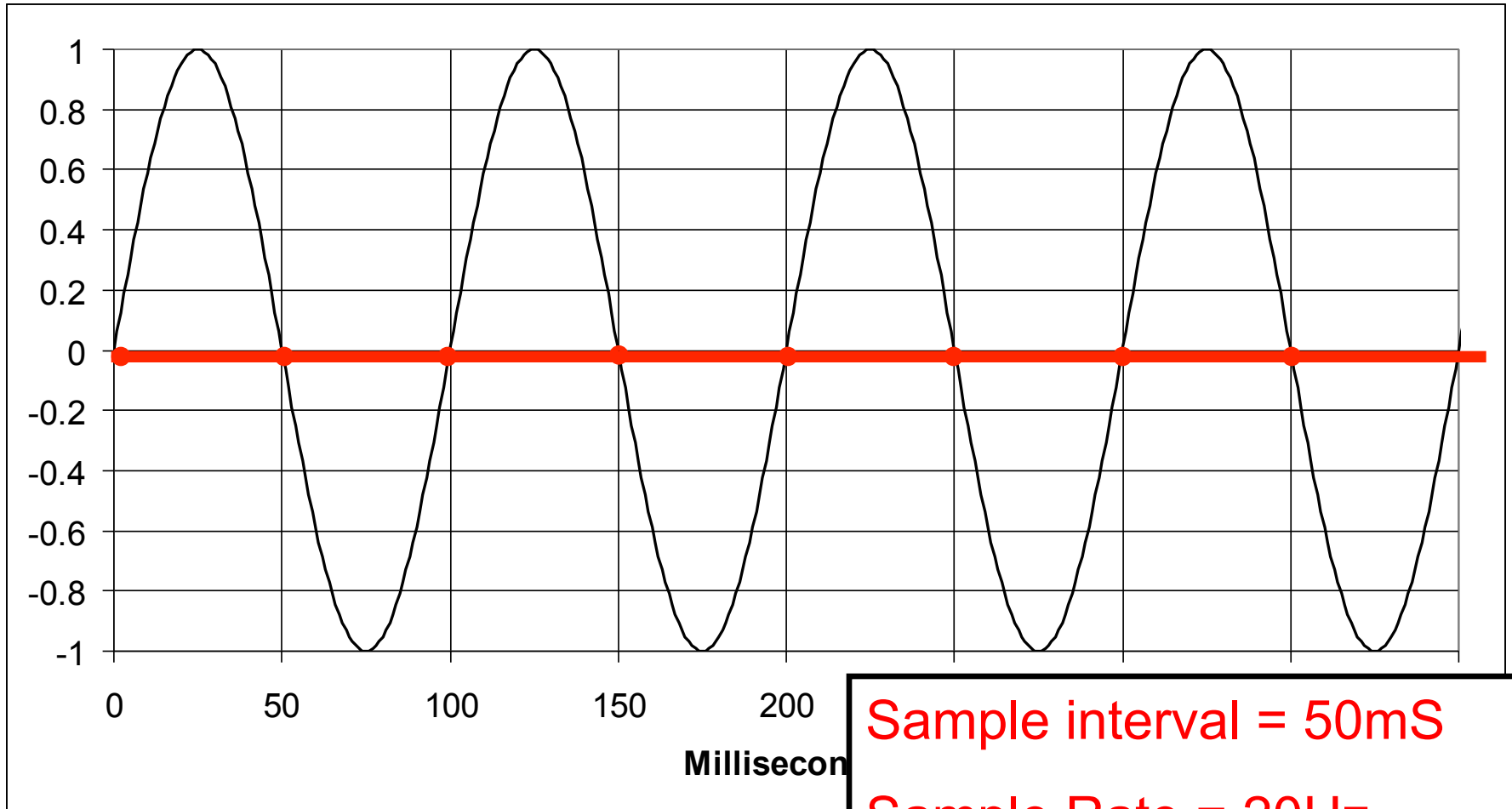


Sample interval = 50mS
Sample Rate = 20Hz

$$f_F = 10Hz$$

$$f_S = 20Hz$$

Discrete Sampling at 20Hz



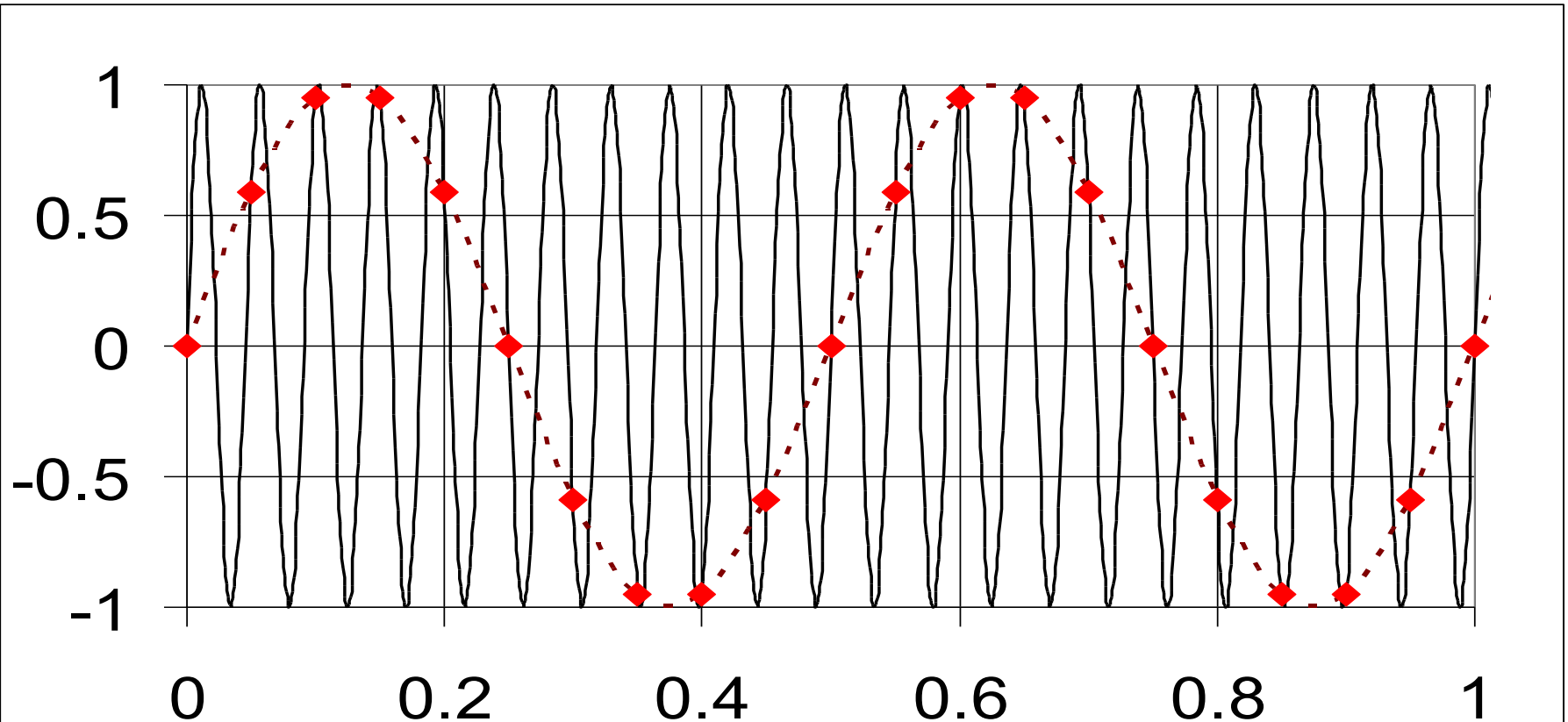
Sample interval = 50mS

Sample Rate = 20Hz

$$f_F = 10Hz$$

$$f_S = 20Hz$$

Aliasing



Original Signal

$$f_F = 18Hz$$

Sample Freq.

$$f_S = 20Hz$$

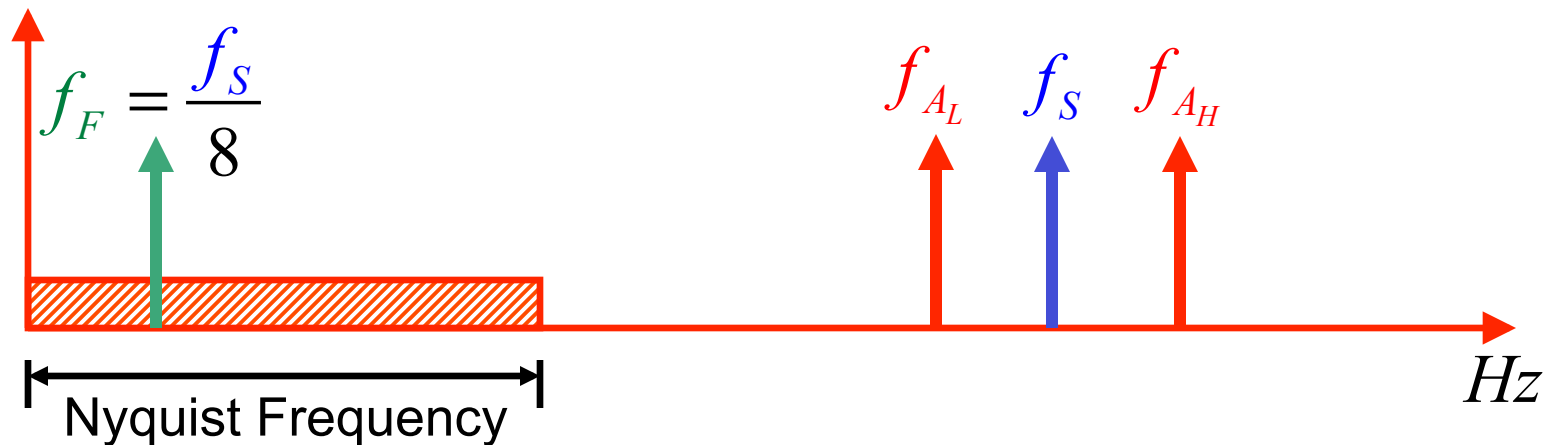
Sample Period

$$T_S = 50mS$$

Aliasing in the Frequency Domain

The frequency of aliased signals is the difference between and sum of the sampling frequency f_S and signal being sampled, f_F . These aliased signals repeat around each integer multiple of the sampling frequency.

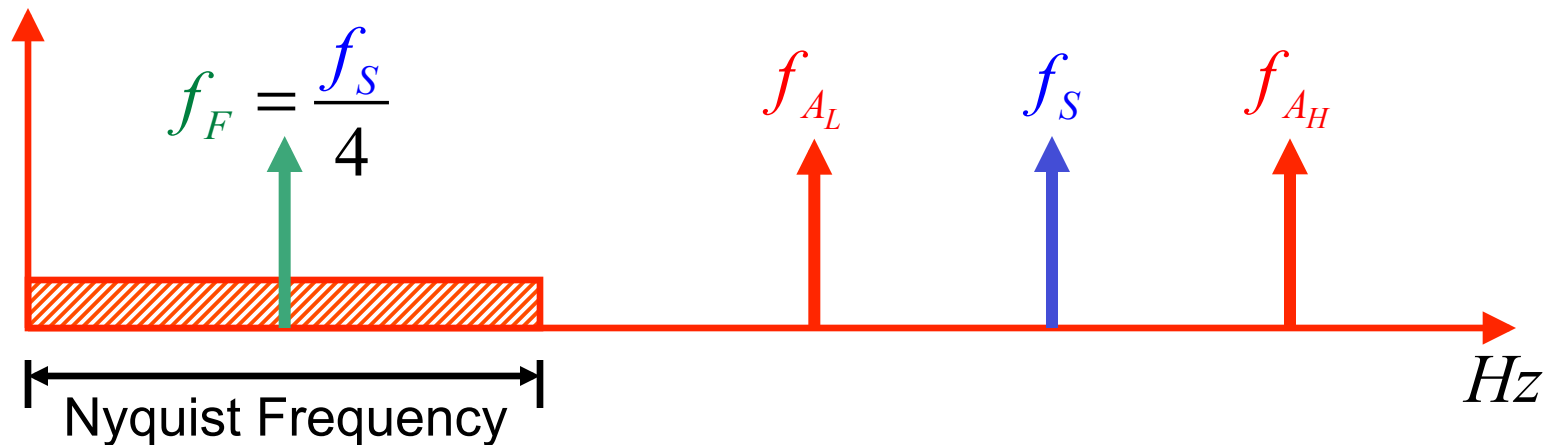
$$f_{A_L} = f_S - f_F \text{ and } f_{A_H} = f_S + f_F$$



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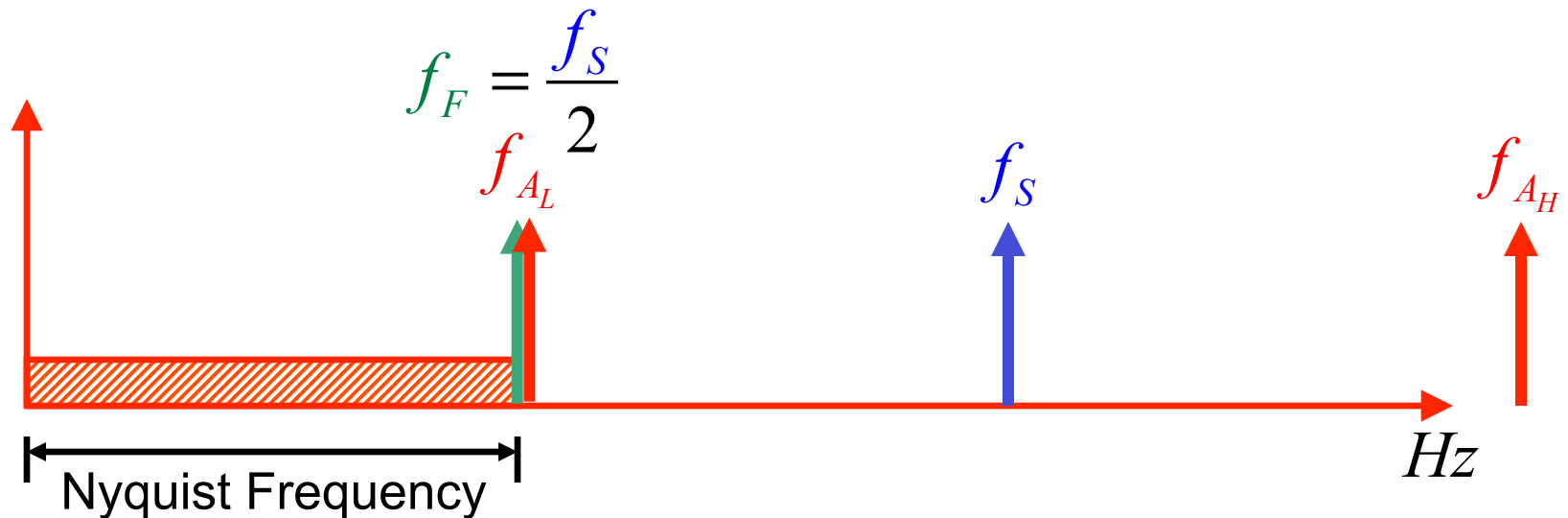
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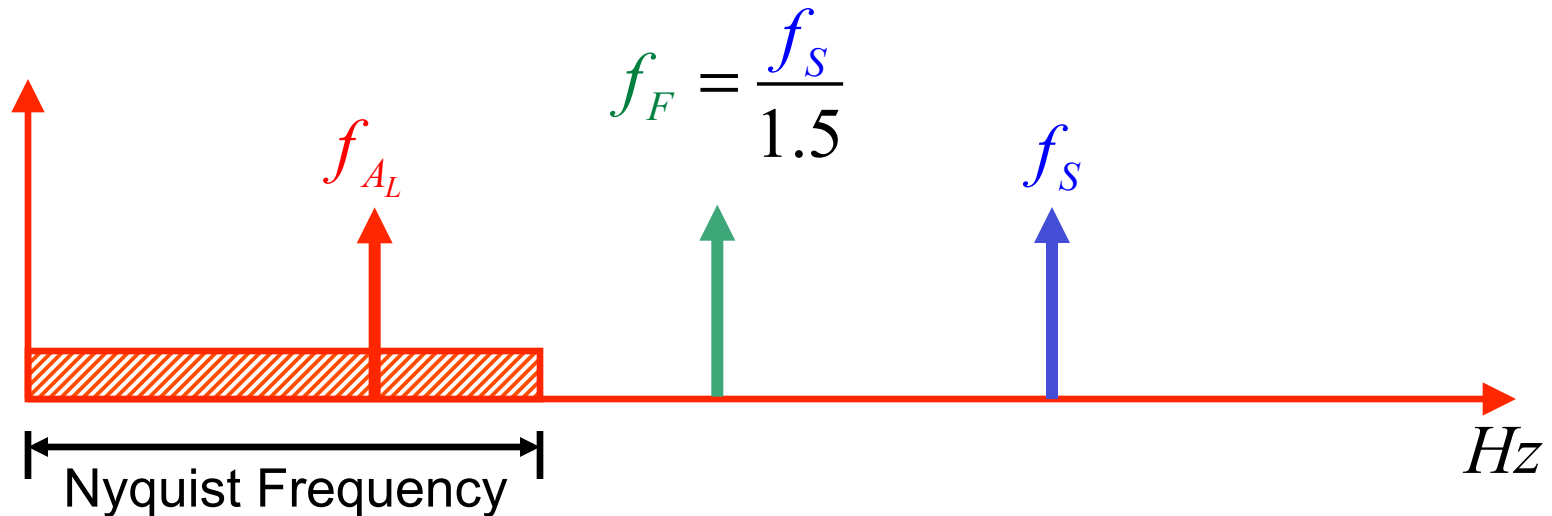
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$$f_{A_L} = f_S - f_F \text{ and } f_{A_H} = f_S + f_F$$



Digital to Analog Converter (DAC) Terminology

Number of Bits, N:

A DAC with N bits provides 2^N discrete output steps.

Resolution, ΔV :

Also known as the “step size”, represents the minimum change in output voltage.

Output Range:

Difference between the maximum and minimum output voltages, usually $(2^N - 1)\Delta V$.

Dynamic Range:

Output Range divided by Resolution or Noise Voltage (whichever gives the *smaller* dynamic range). If noise is smaller than ΔV , then dynamic range is $2^N - 1$.

In-Class Exercise

A 10-bit DAC is set up to output a DC voltage from -12V to +12V. Determine the resolution.

The 10 bits produce a total of $2^{10} = 1024$ steps.

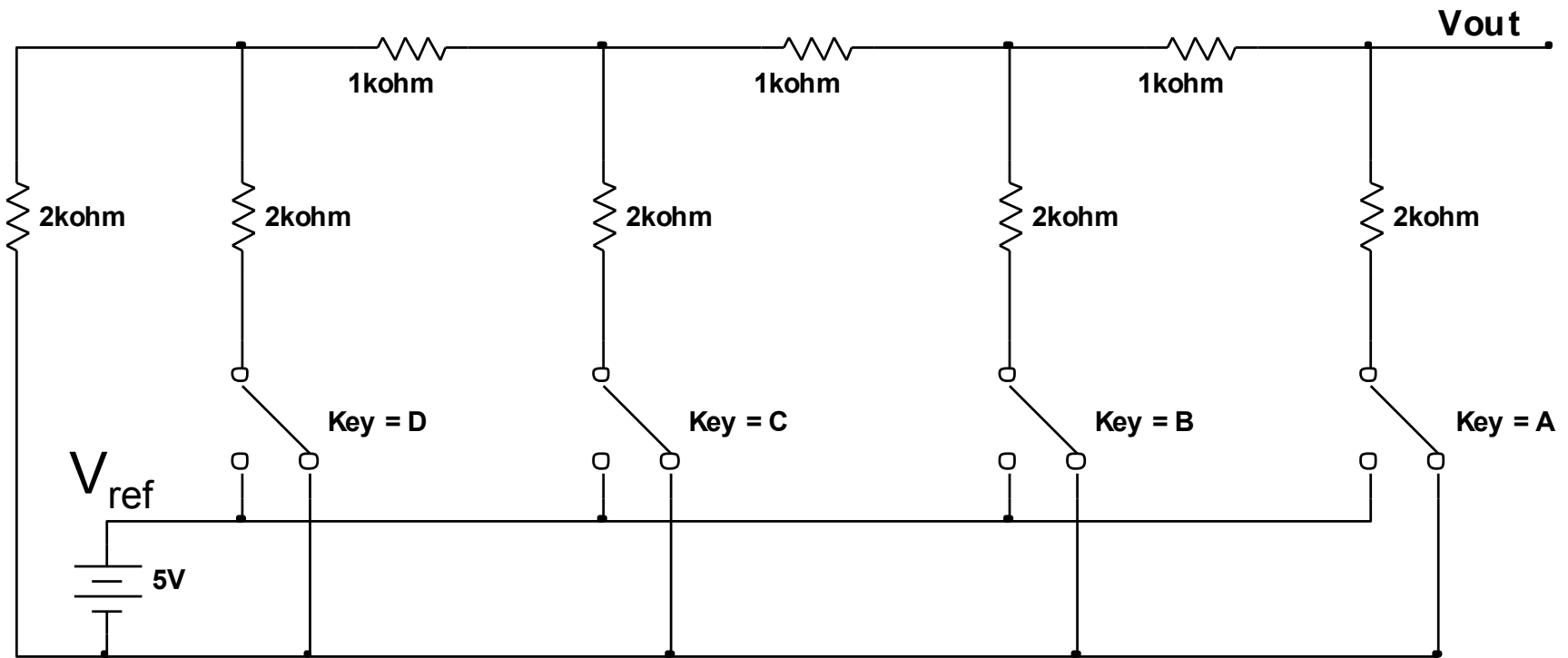
The range is $+12V - (-12V) = +24V$.

Therefore the resolution is $24V/1023 = 0.02346V$.

23.5mV/step



One Approach to DAC: R-2R Ladder Circuit

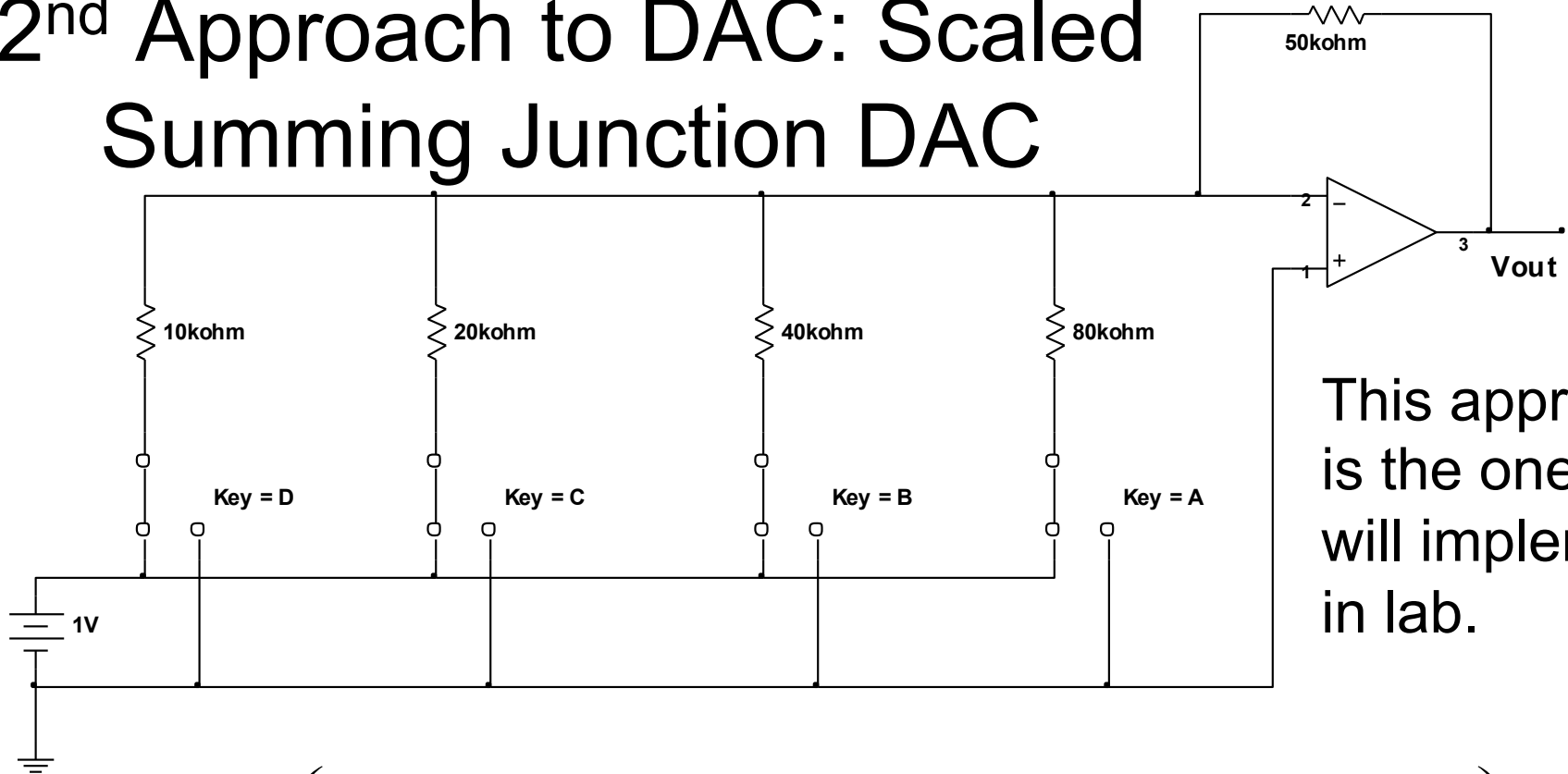


$$V_{out} = 5V \cdot \left(\frac{A}{2^1} + \frac{B}{2^2} + \frac{C}{2^3} + \frac{D}{2^4} \right)$$

What is V_{max} ?

$$V_{max} = V_{ref} \cdot 15/16 = 4.69V \quad V_{min} = 0$$

2nd Approach to DAC: Scaled Summing Junction DAC



This approach is the one we will implement in lab.

$$V_{out} = -1V \cdot \left(\frac{A \cdot 50k\Omega}{80k\Omega} + \frac{B \cdot 50k\Omega}{40k\Omega} + \frac{C \cdot 50k\Omega}{20k\Omega} + \frac{D \cdot 50k\Omega}{10k\Omega} \right)$$

$$= -10 \cdot \left(\frac{A}{2^4} + \frac{B}{2^3} + \frac{C}{2^2} + \frac{D}{2^1} \right) V$$

What is Range?

$$V_{max} = 0, V_{min} = -10V \cdot 15/16 = -9.38V$$

$$\text{Range} = 9.38V$$

Analog to Digital Converter (ADC) Terminology

Number of Bits:

An ADC with N bits divides the input range into 2^N discrete steps. For example, an 8 bit ADC can produce a total of 256 different output codes.

Full Scale Input Range

Difference between the minimum and maximum input voltage that can be measured.

Resolution:

Quantization, also known as the “step size”, is the change in input voltage represented by each increment of the output. Often referred to as LSB (least significant bit)

Dynamic Range:

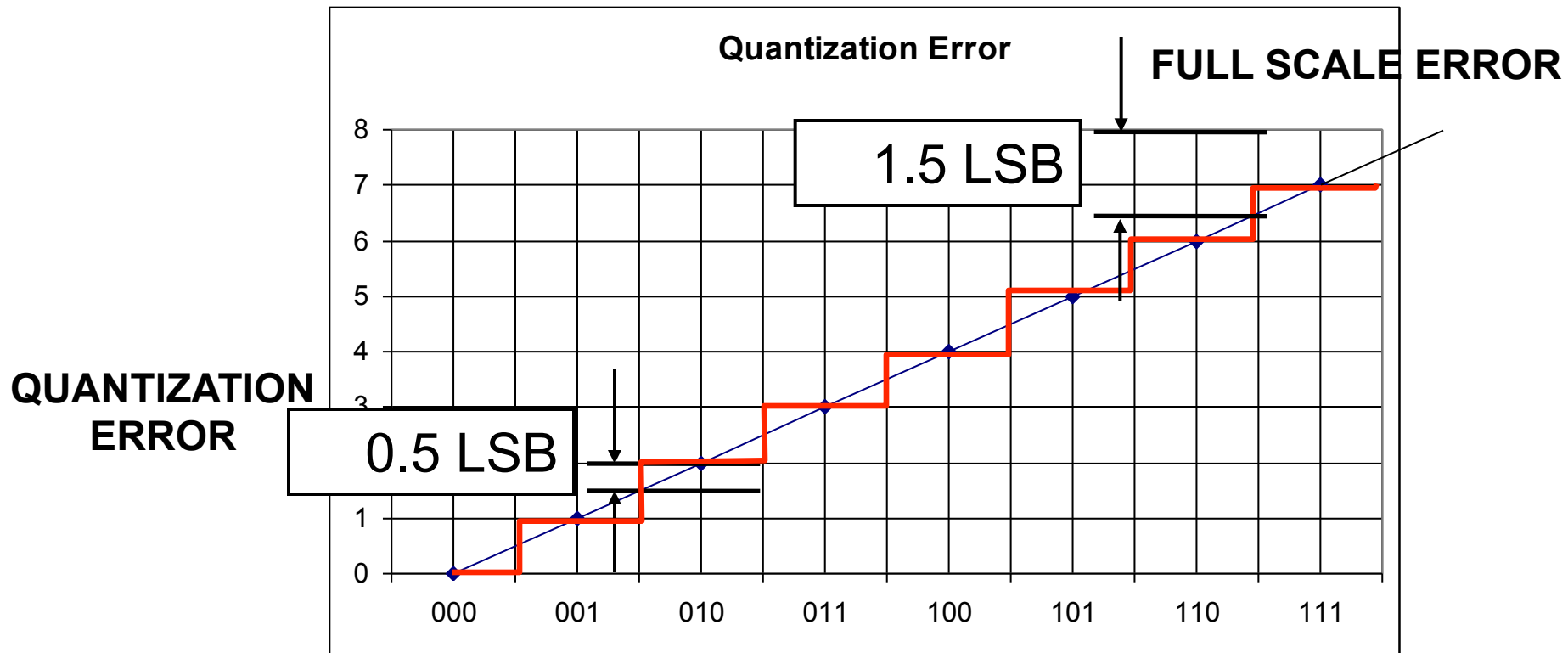
Input Range divided by resolution or noise. Typically equals $2^N - 1$, if noise is less than LSB.

ADC Accuracy

- **QUANTIZATION ERROR** Inherent accuracy ($\pm 1/2\text{LSB}$, least significant bit)
- **INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from zero scale or negative full scale ($1/2$ LSB below the first code transition) through positive full scale ($1/2$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.
- **DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB. DNL is commonly measured at the rated clock frequency with a ramp input.
- **MISSING CODES** are output codes that are skipped or never appear at the ADC outputs. These codes cannot be reached by any input value.
- **OFFSET ERROR** is the difference between the ideal and actual LSB transition point.
- **FULL SCALE ERROR** is how far the last code transition is from the ideal 1.5 LSB below positive V_{ref} (V_{ref} is 2^N times step size)
- **GAIN ERROR** is number of LSB “gained” from conversion from lowest to highest output. It is a measure of the deviation of the ADC from linear (gain = 1) conversion.

See figure 9.44 in H&H page 615

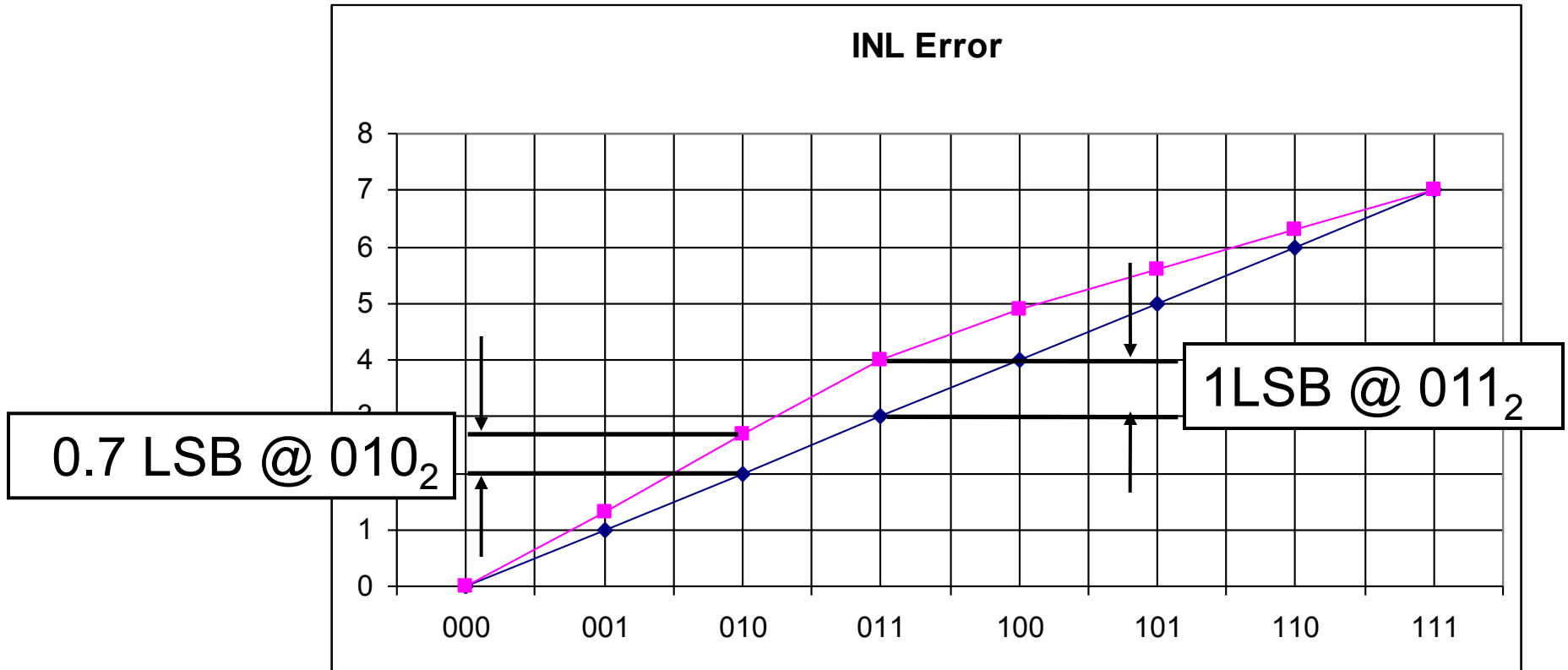
Ideal ADC: Quantization Error



-*Quantization error* is the inherent deviation of the output from a straight line.

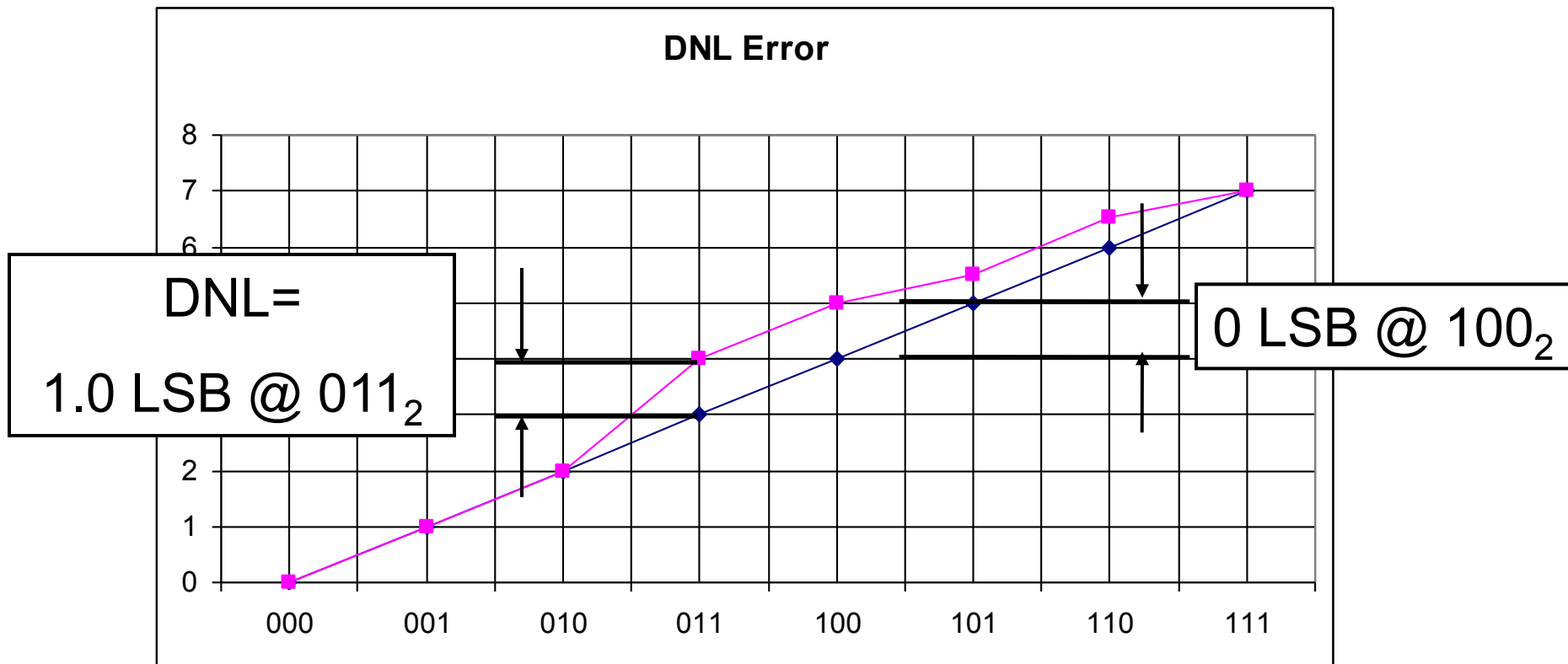
-Note last transition is 1.5 LSB from V_{ref} (used to measure full scale error)

Sampled System Errors - INL



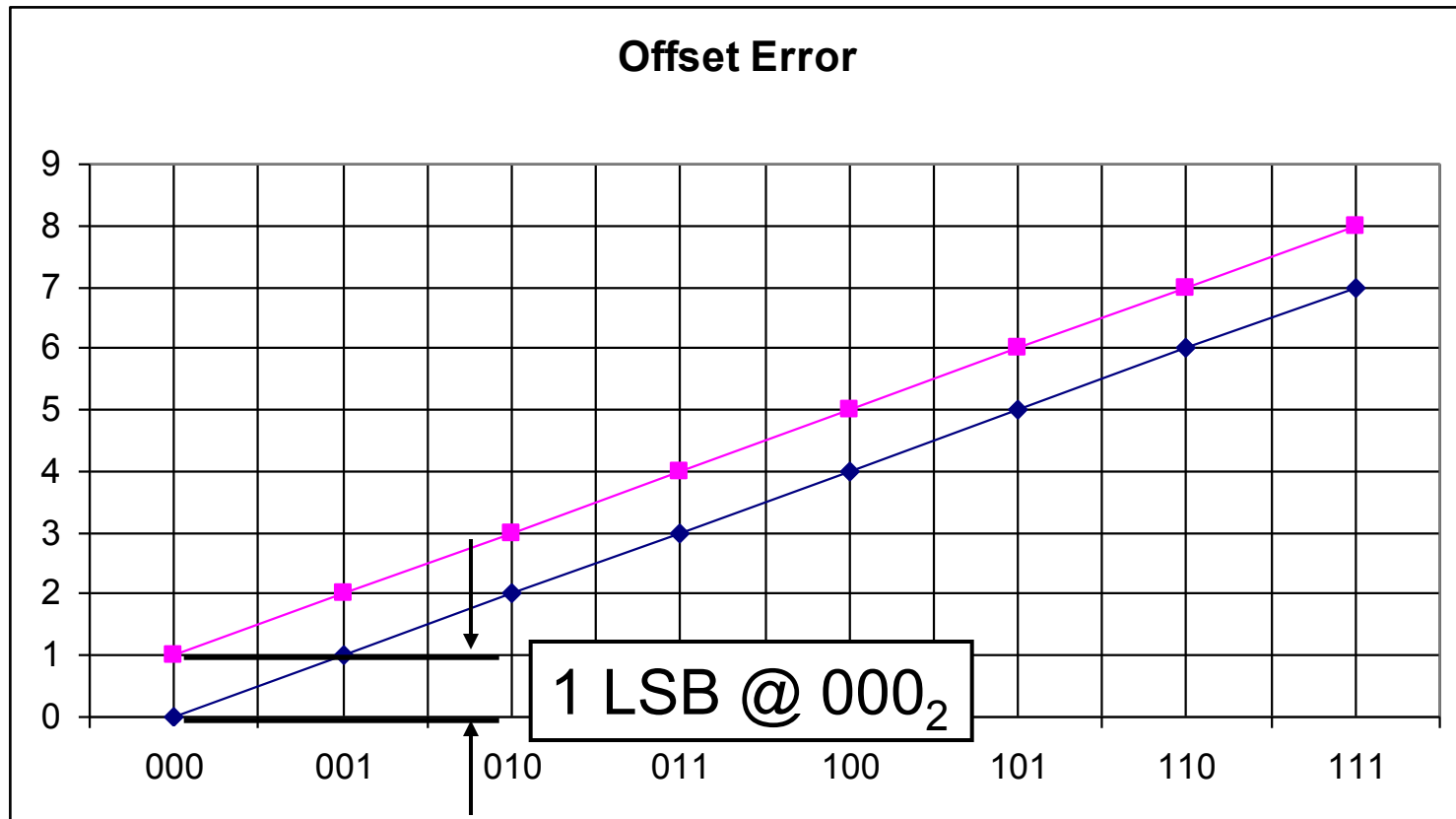
Integral Non-Linearity is the deviation of the output from a straight line.

Sampled System Errors - DNL



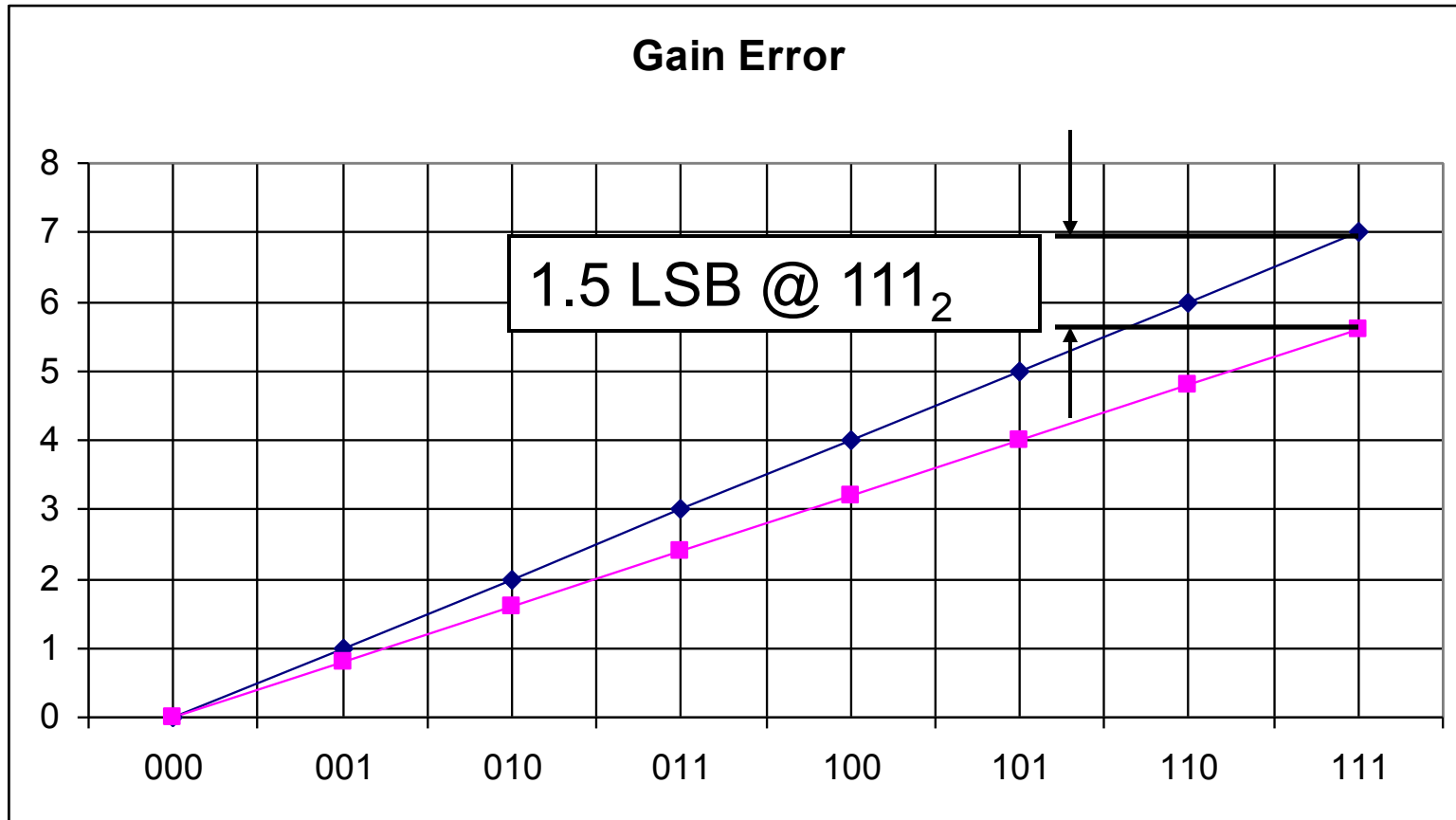
Differential Non-Linearity is the maximum difference between the expected stepsize (1 LSB) and that steps actually produced by the DAC.

Sampled System Errors - Offset



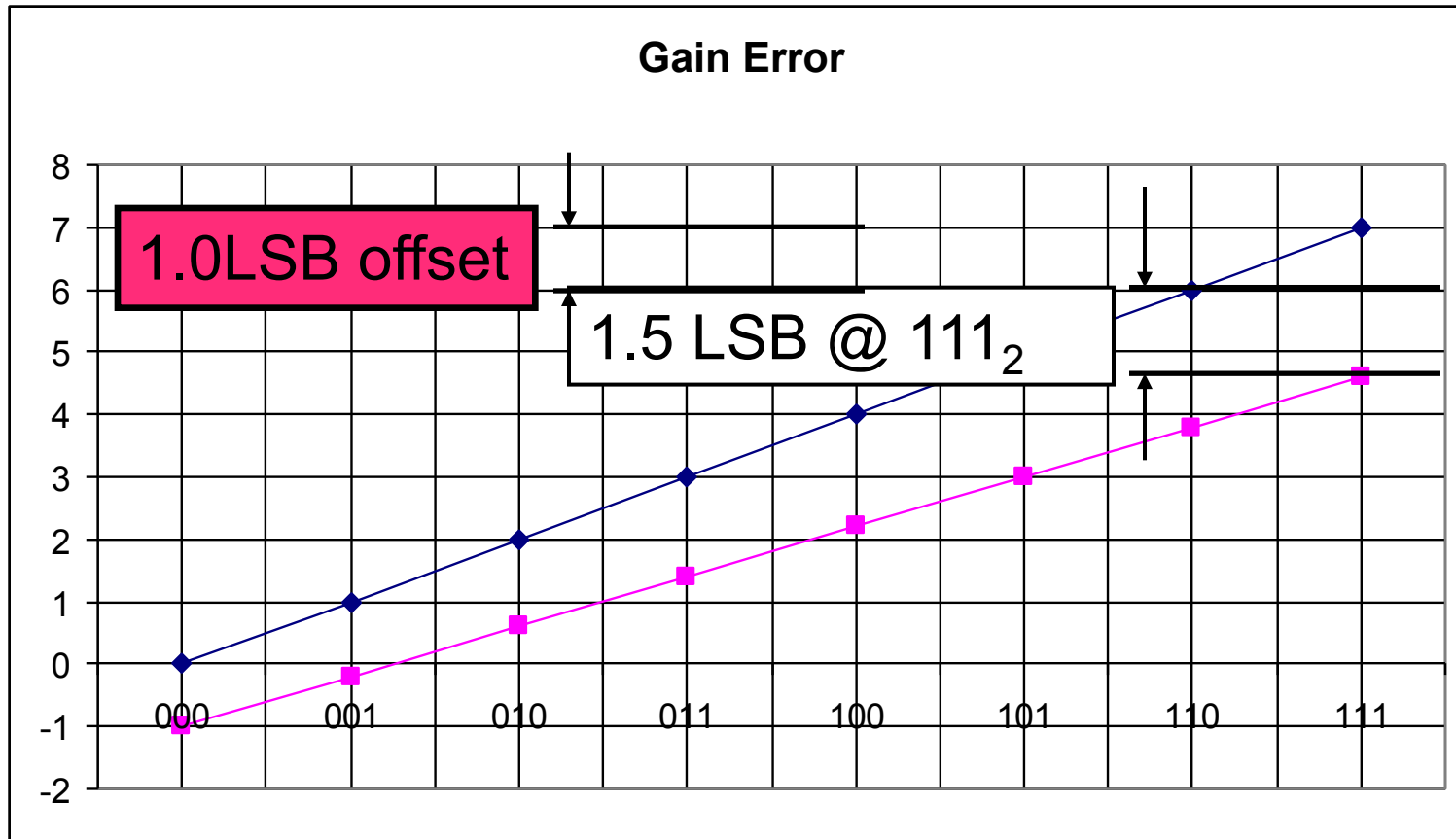
Offset Error is measured at 000₂.

Sampled System Errors - Gain



Gain Error is measured at 111_2 . The offset error must be known to compute this value. ($y=mx+b$)

Sampled System Errors - Gain



Gain Error is measured at 111_2 . The offset error must be known to compute this value. ($y=mx+b$)

References

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2. Analog Devices, “Fundamentals of Sampled Data Systems”, accessed MAR 2008
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