

# Today

**3/8/11 Lecture 8**

## **Sequential Logic, Clocks, and Displays**

- **Flip Flops and Ripple Counters**
- **One Shots and Timers**
- **LED Displays, Decoders, and Drivers**

## **Homework**

- **XXXX**

## **Reading**

- **H&H sections on sequential logic and clocks.**

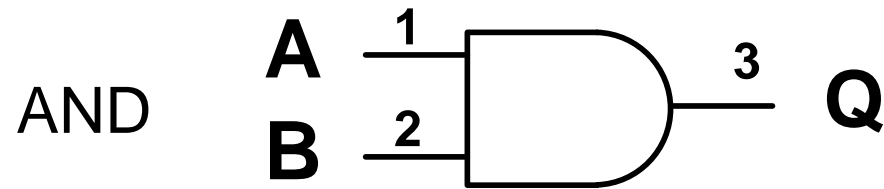
## **Lab**

- **If you have questions:  
Email or call me on my cell (up to 10pm)**

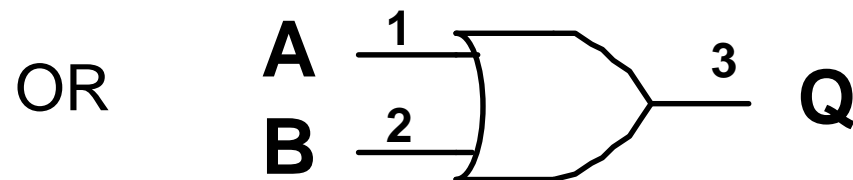
# Review of Logic Gates

Schematic symbol

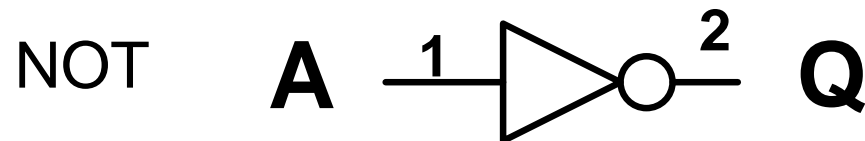
Algebraic example



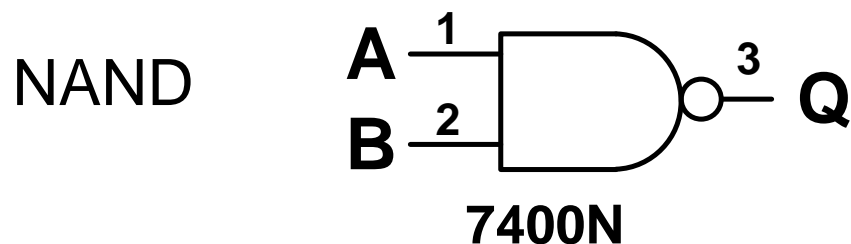
$$Q = A \cdot B$$



$$Q = A + B$$



$$Q = \overline{A}$$



$$\overline{A \cdot B} = Q$$

# Combinational versus Sequential

## Combinational logic:

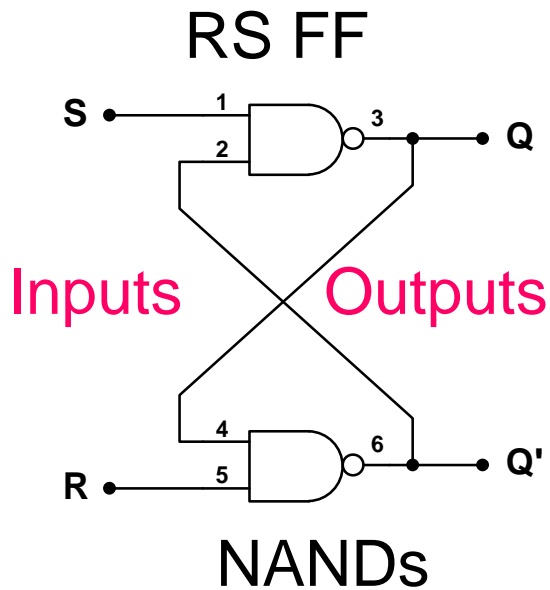
Output state of the circuit is dependant only on the present input states.

## Sequential Logic:

Output state depends on both the present input states *and* on previous history.

*A Sequential Logic circuit has memory!*

# RS Flip-Flop



This circuit cannot be analyzed combinatorially. The output is determined by considering these NAND functions temporally, that is, discussing the state of the outputs ( $Q_1$  and  $Q'_1$ ) after some event in terms of ( $Q_0$  and  $Q'_0$ ) before.

$$Q_1 = \overline{S \cdot Q'_0} \quad \text{and} \quad Q'_1 = \overline{R \cdot Q_0}$$

*if*  $S = 1$  *and*  $R = 1$

*then*  $Q_1 = \overline{S \cdot Q'_0} = \overline{Q'_0}$

*and*  $Q'_1 = \overline{R \cdot Q_0} = \overline{Q_0}$

If  $Q'_0 = \text{NOT}(Q_0)$ , then state is unchanged.

The state only changes when one of the inputs (R or S, but not both) are briefly toggled low (FALSE).

# State Table for RS FF

Toggle "Set" input (with R=1)

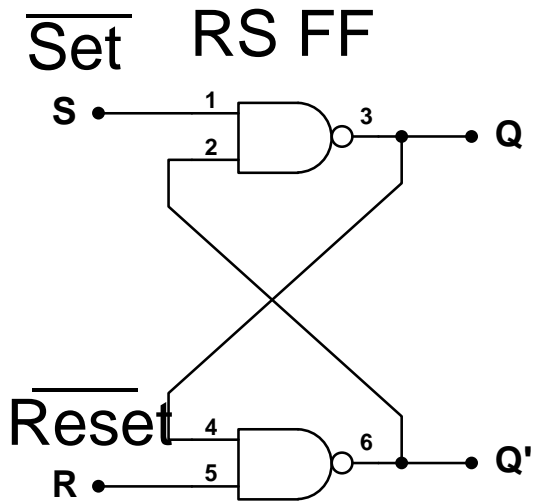
S	Q' <sub>0</sub>	Q <sub>1</sub>	$\overline{R \cdot Q_1}$	Q' <sub>1</sub>
0	0	1	0	0
0	1	1	0	0
1	0	1	0	0
1	1	0	1	1

}

Q is "set" high if S goes low

}

No change if both high



Toggle "Reset" input (with S=1)

R	Q <sub>0</sub>	Q' <sub>1</sub>	$\overline{S \cdot Q'_1}$	Q <sub>1</sub>
0	0	1	0	0
0	1	1	0	0
1	0	1	0	0
1	1	0	1	1

}

Q is "reset" low if R goes low

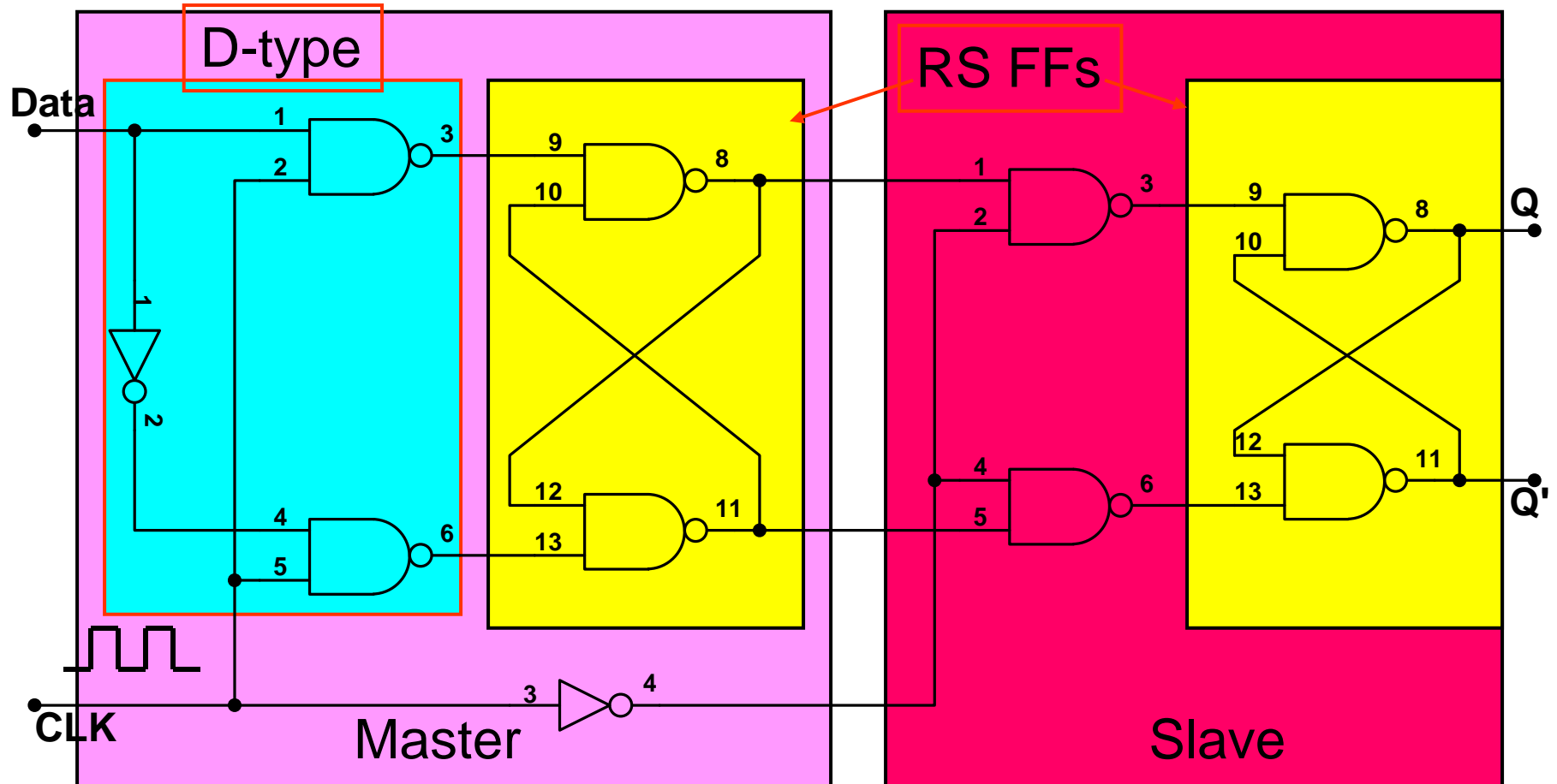
}

No change if both high

*State Table*

S	R	Q	Q'
0	0	?	?
0	1	1	0
1	0	0	1
1	1	No Change	

# D-type Master-Slave Clocked Flip-Flop



Operation:

$Q=D$  and  $Q'=\text{not}(D)$  when CLK goes high.

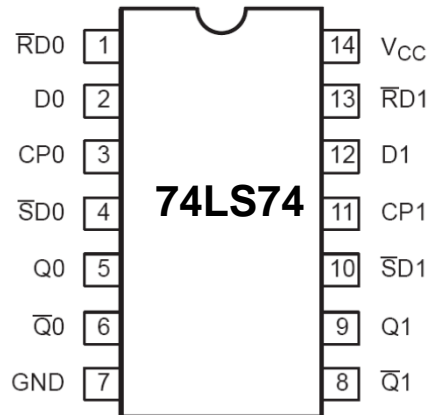
No change when CLK is low or goes low, even if D changes

No change if D changes after CLK goes high

Data is clocked and locked when CLK transition from low to high

(Details: [http://www.piclist.com/images/www/hobby\\_elec/e\\_ckt10\\_6.htm](http://www.piclist.com/images/www/hobby_elec/e_ckt10_6.htm))

# 74LS74 Chip-Dual D-type flip-flop with Set and Reset

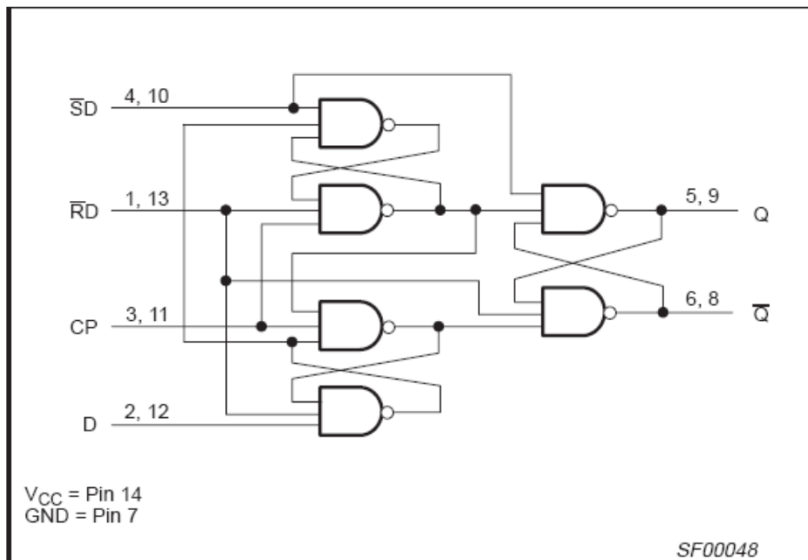


FUNCTION TABLE

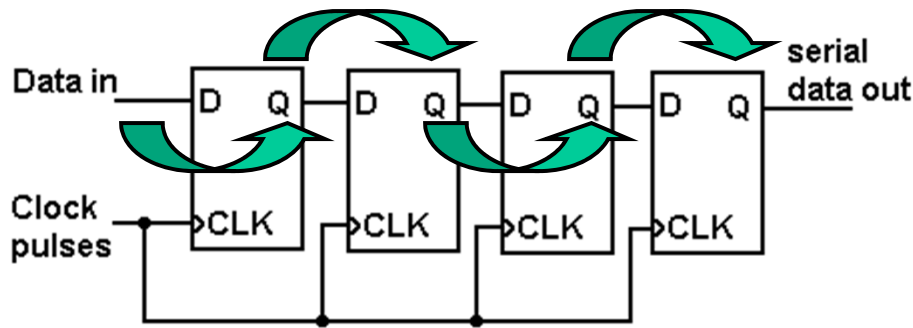
	INPUTS				OUTPUTS		OPERATING MODE
	$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
	L	H	X	X	H	L	Asynchronous set
	H	L	X	X	L	H	Asynchronous reset
	L	L	X	X	H	H	Undetermined*
$\nearrow$	H	H	$\uparrow$	h	H	L	Load "1"
$\searrow$	H	H	$\uparrow$	l	L	H	Load "0"
$\sim$	H	H	$\nabla$	X	NC	NC	Hold

NOTES:

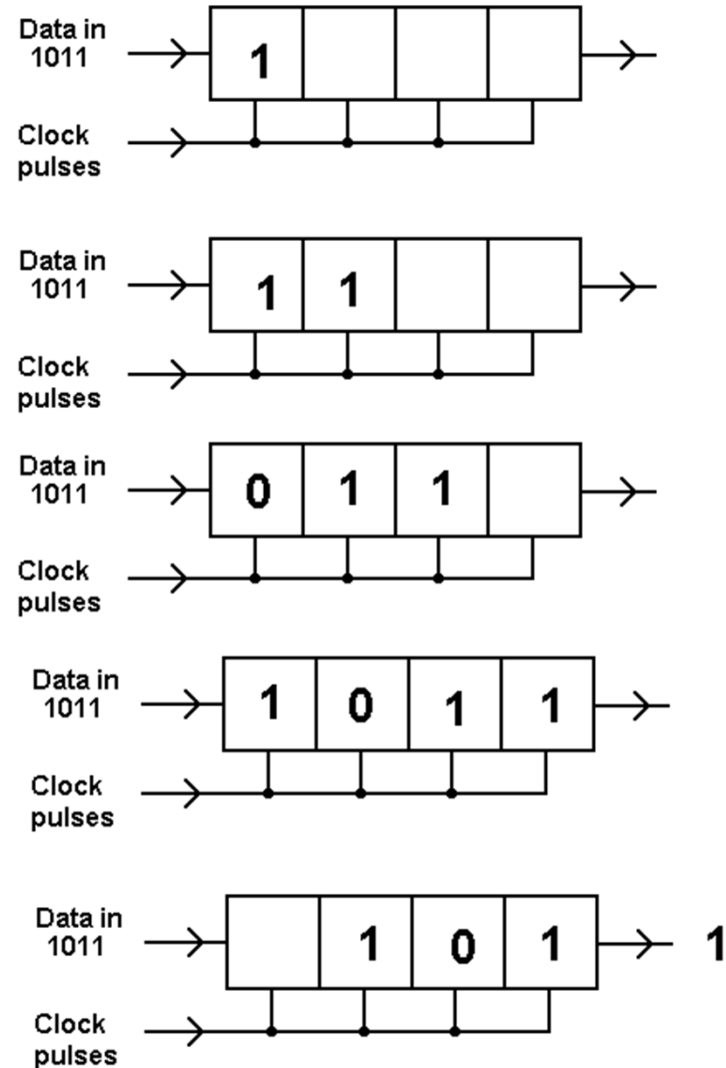
- H = High voltage level
- h = High voltage level one setup time prior to low-to-high clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to low-to-high clock transition
- NC = No change from the previous setup
- X = Don't care
- $\uparrow$  = Low-to-high clock transition
- $\nabla$  = Not low-to-high clock transition
- \* = This setup is unstable and will change when either set or reset return to the high level.



# Flip – Flop Shift Register

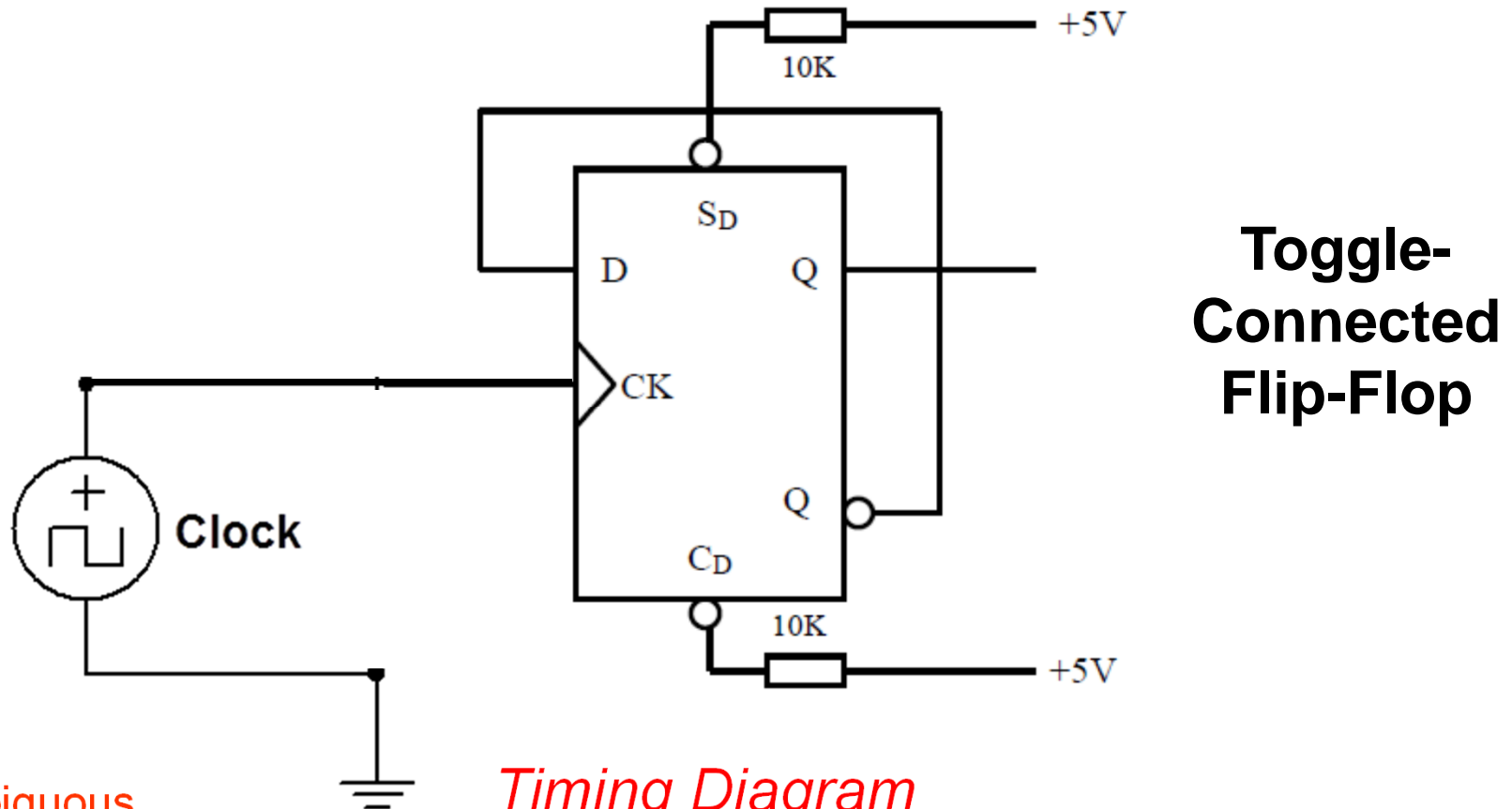


“1011” is clocked in one bit at a time

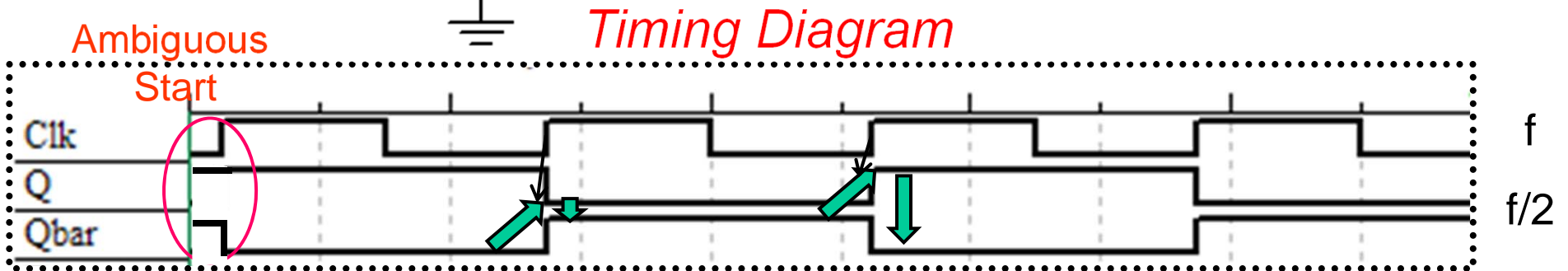




# Clocked Flip-Flop: Divide by 2



**Toggle-  
Connected  
Flip-Flop**

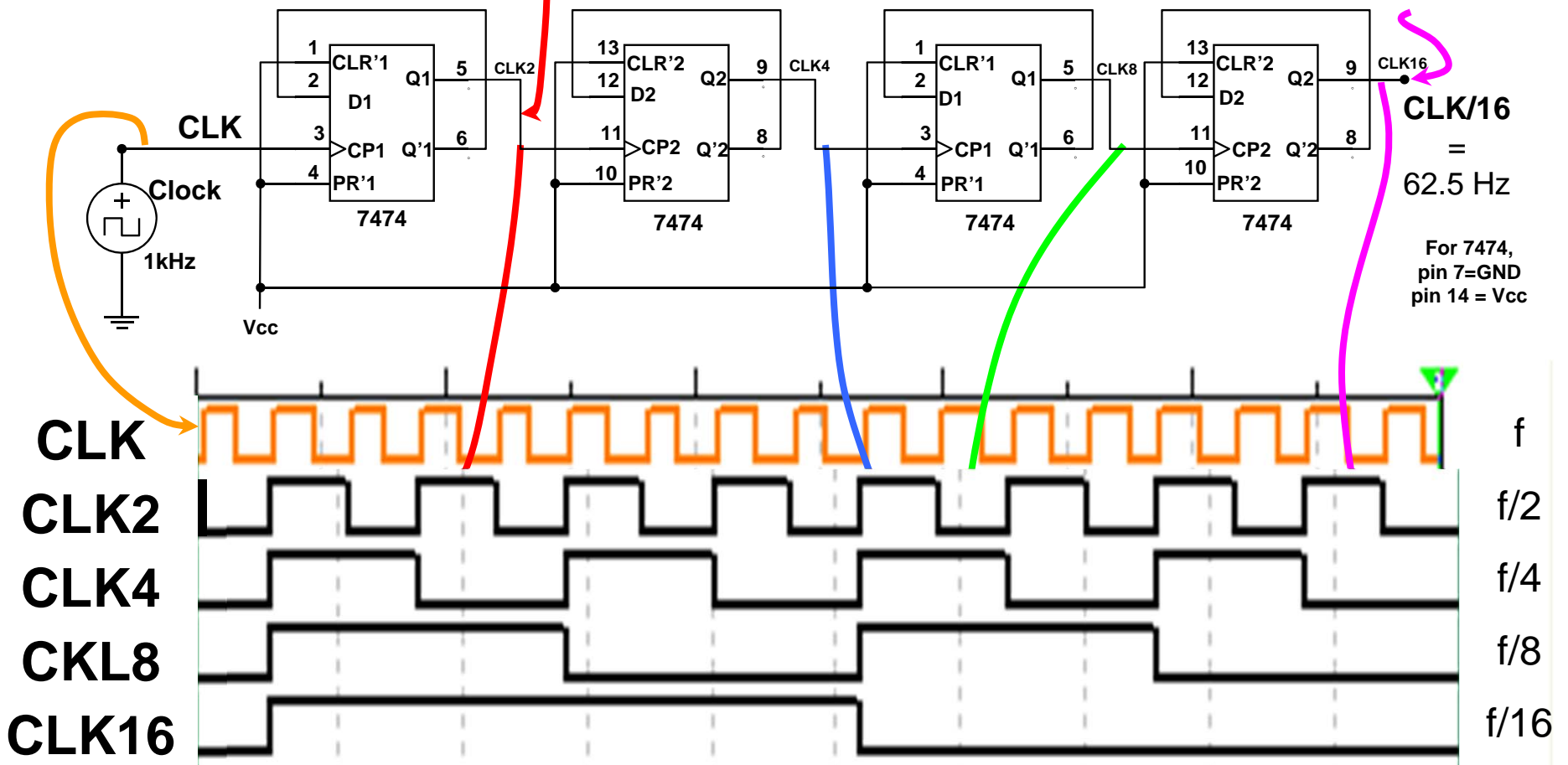


# Ripple Counter

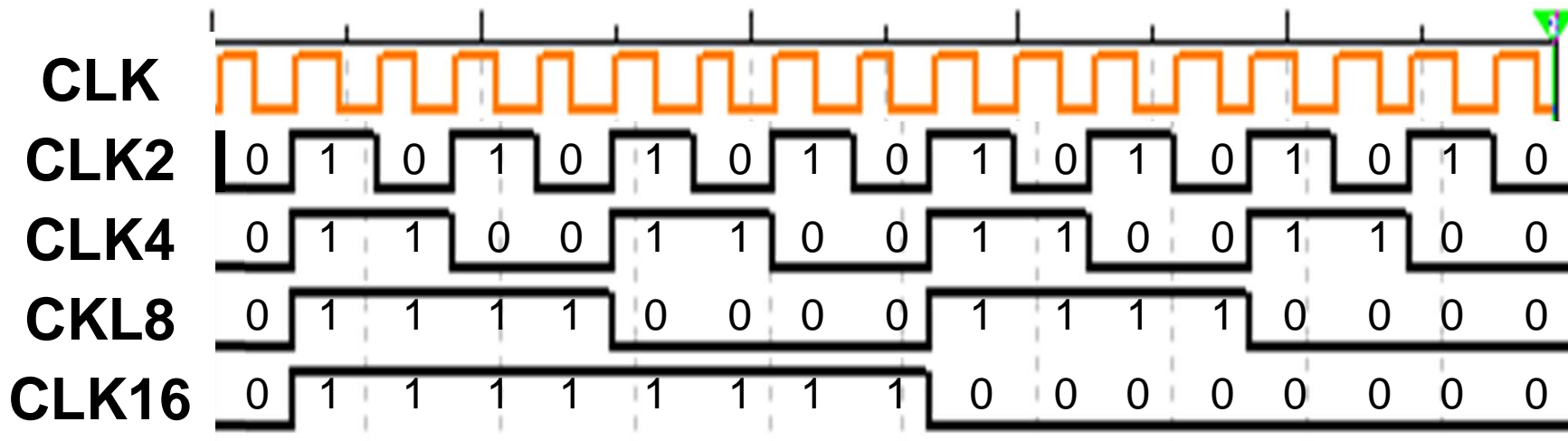
Clock plus  
 $n$  flip-flops

Divided by 2

Divided by  $2^n$

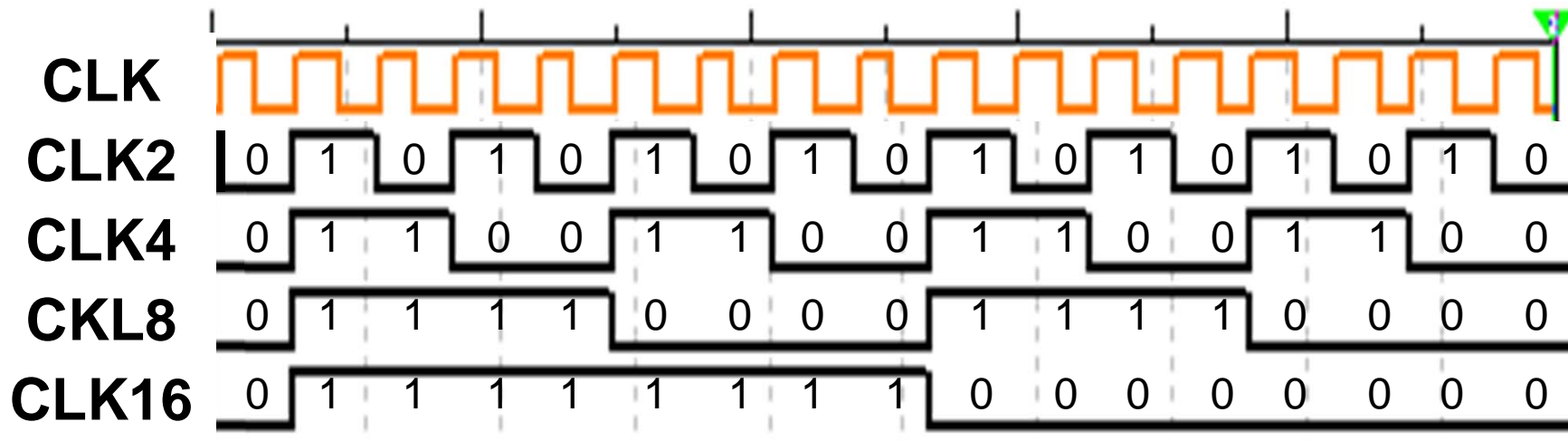


# Ripple Down Counter



Q0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Q1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Q2	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Q3	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Hex	0	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

# Ripple Up Counter



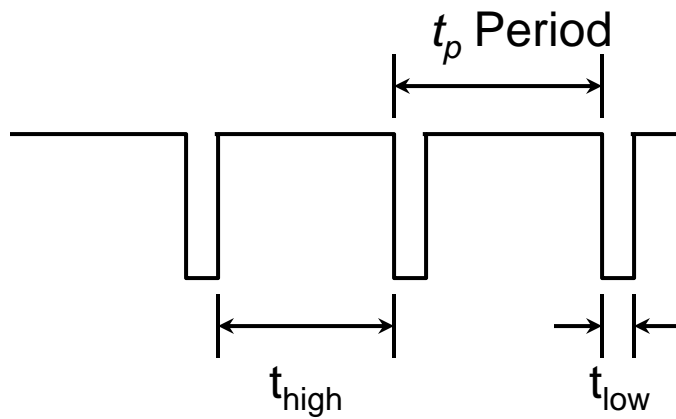
$\overline{Q0}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$\overline{Q1}$	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
$\overline{Q2}$	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
$\overline{Q3}$	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Hex	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

# Astable Multivibrator

The astable multivibrator is an oscillator.

The *period and duty cycle* are properties of oscillator.

$$f = \frac{1}{t_p} \text{ in Hertz}$$



Depending on whose definition you use

$$\% \text{Duty Cycle High} = \frac{t_{high}}{t_p} \cdot 100$$

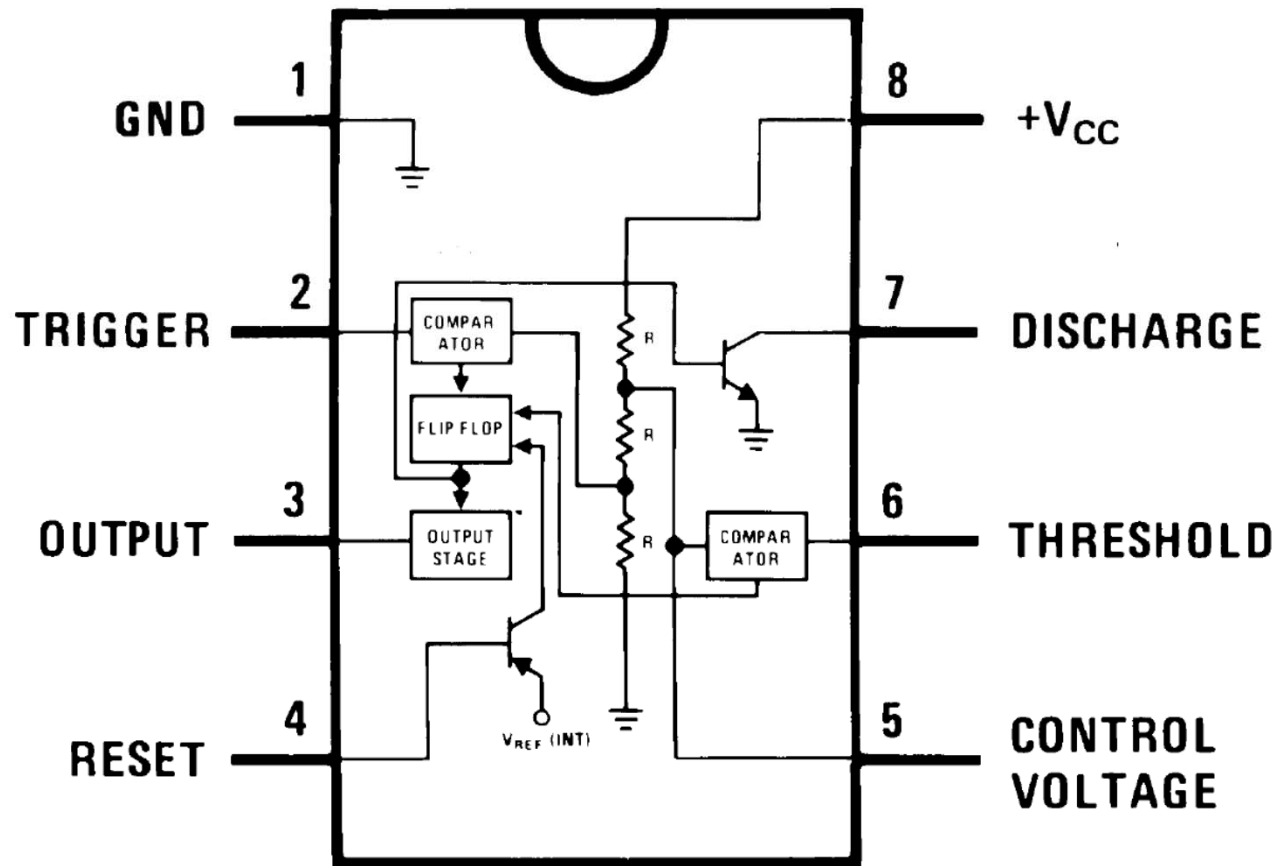
OR

$$\% \text{Duty Cycle Low} = \frac{t_{low}}{t_p} \cdot 100$$

$$t_p = t_{high} + t_{low}$$

# Timer Circuits - 555

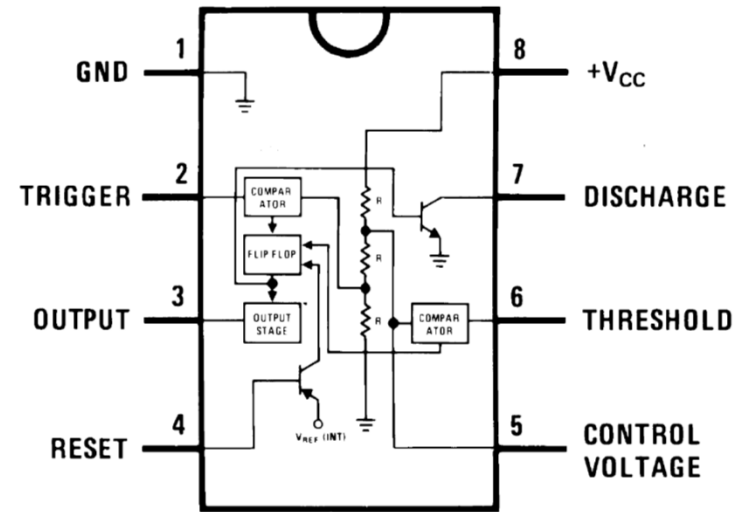
Dual-In-Line, Small Outline  
and Molded Mini Small Outline Packages



# Timer Circuits - 555

FUNCTION TABLE

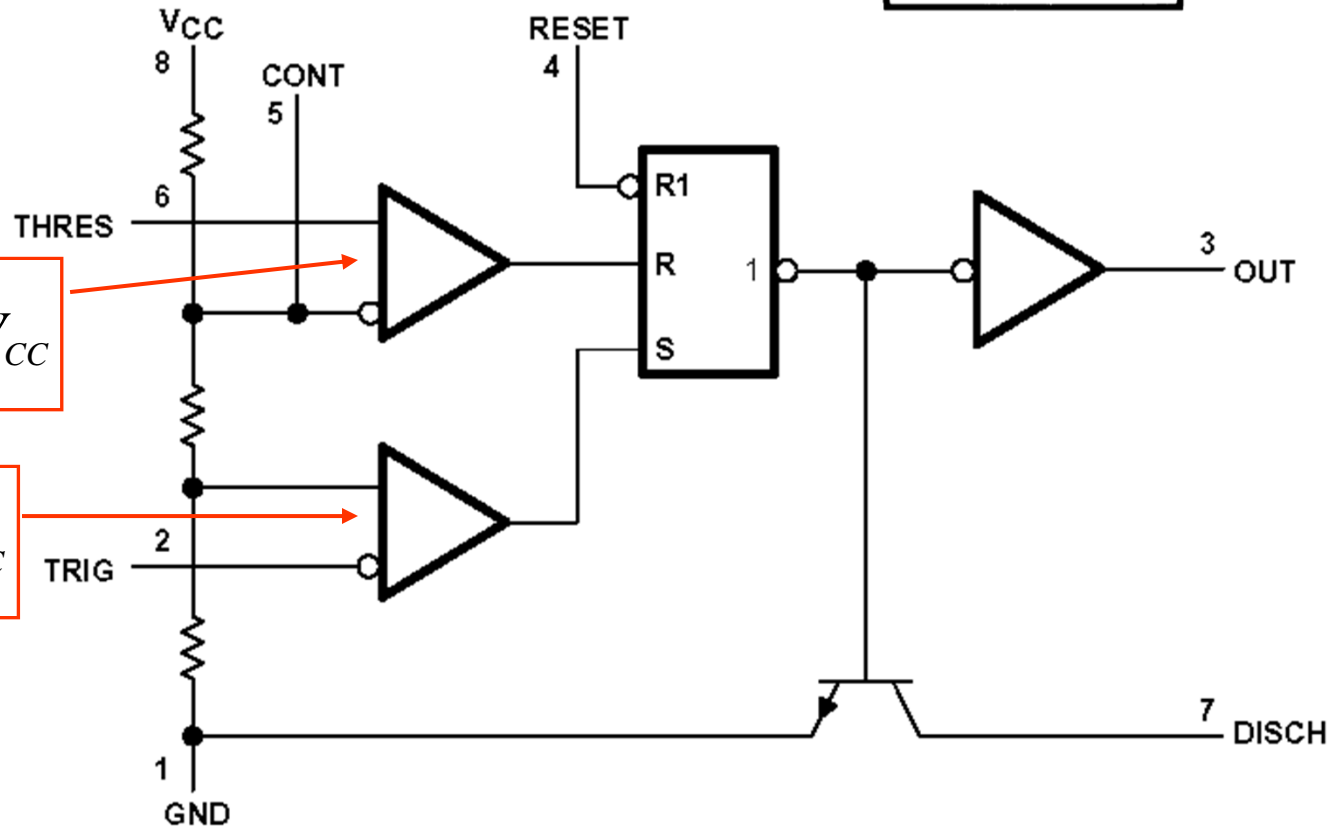
RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$<1/3 V_{DD}$	Irrelevant	High	Off
High	$>1/3 V_{DD}$	$>2/3 V_{DD}$	Low	On
High	$>1/3 V_{DD}$	$<2/3 V_{DD}$	As previously established	



Functional Block Diagram

$$V_{THRES} \triangleq \frac{2}{3} V_{CC}$$

$$V_{TRIG} \triangleq \frac{1}{3} V_{CC}$$

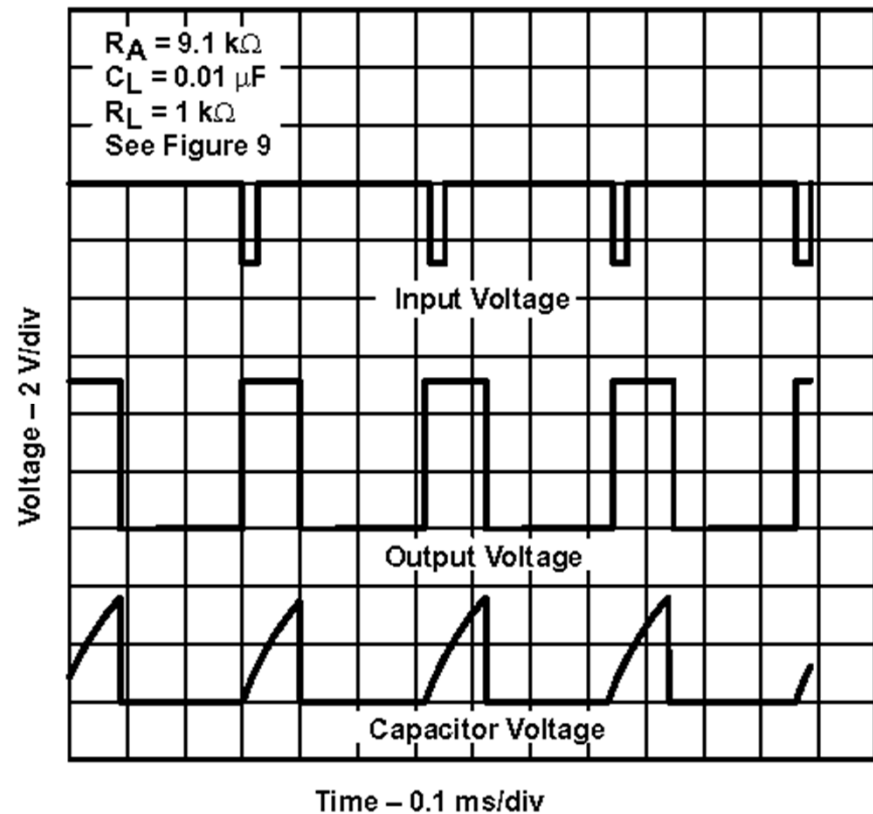
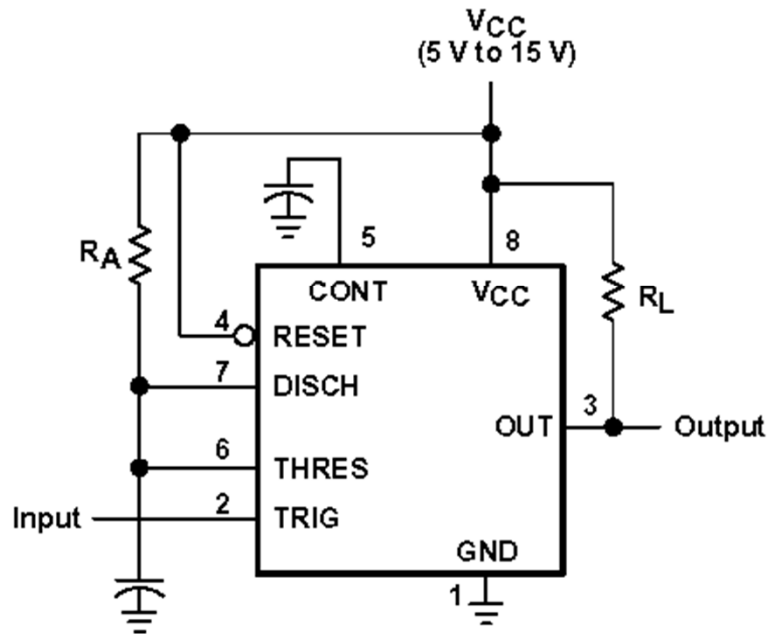


# One Shot with a 555

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< 1/3 V_{DD}$	Irrelevant	High	Off
High	$> 1/3 V_{DD}$	$> 2/3 V_{DD}$	Low	On
High	$> 1/3 V_{DD}$	$< 2/3 V_{DD}$	As previously established	

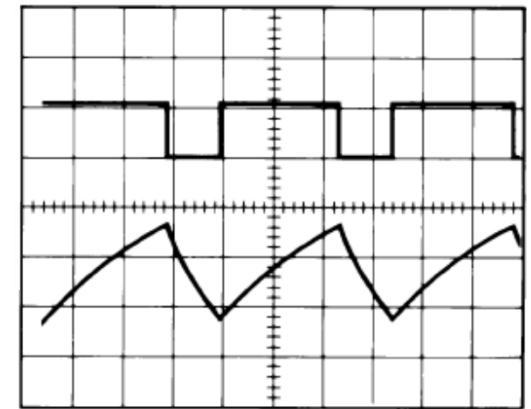
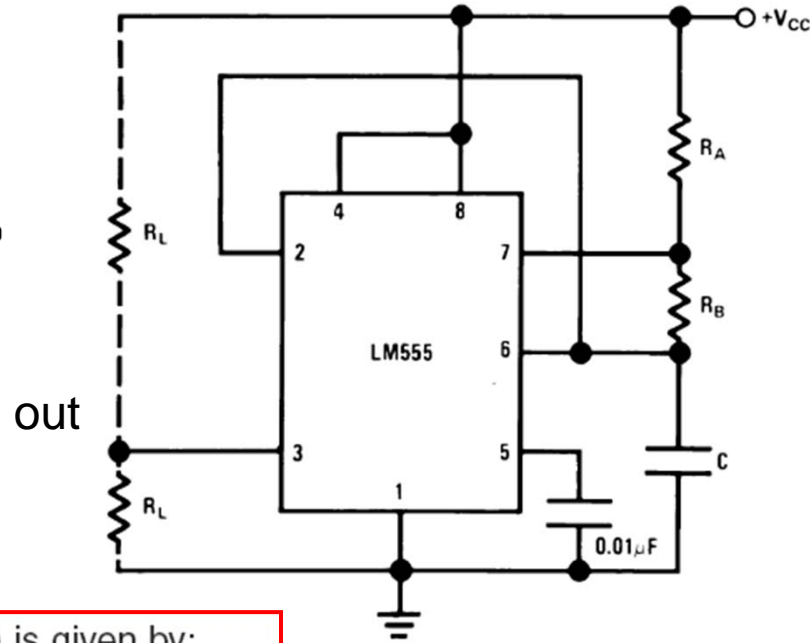
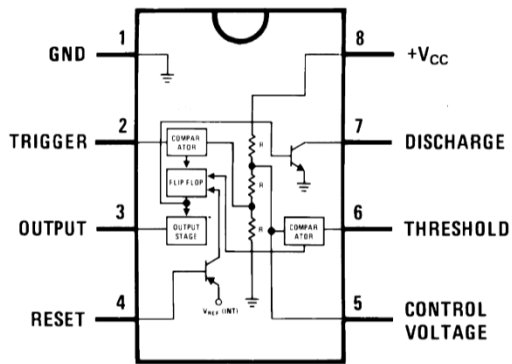
“One shot” per trigger pulse



$$t_w = 1.1R_A C \quad (\text{pulse width from the spec sheet})$$



# Continuous Shots with a 555



00785109

V<sub>CC</sub> = 5V

TIME = 20 μs/DIV.

Top Trace: Output 5V/Div.

Bottom Trace: Capacitor Voltage 1V/Div.

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Low Duty  
Cycle

$$D = \frac{R_B}{R_A + 2R_B} < 50\%$$

# Setting Frequency of a 555 clock

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

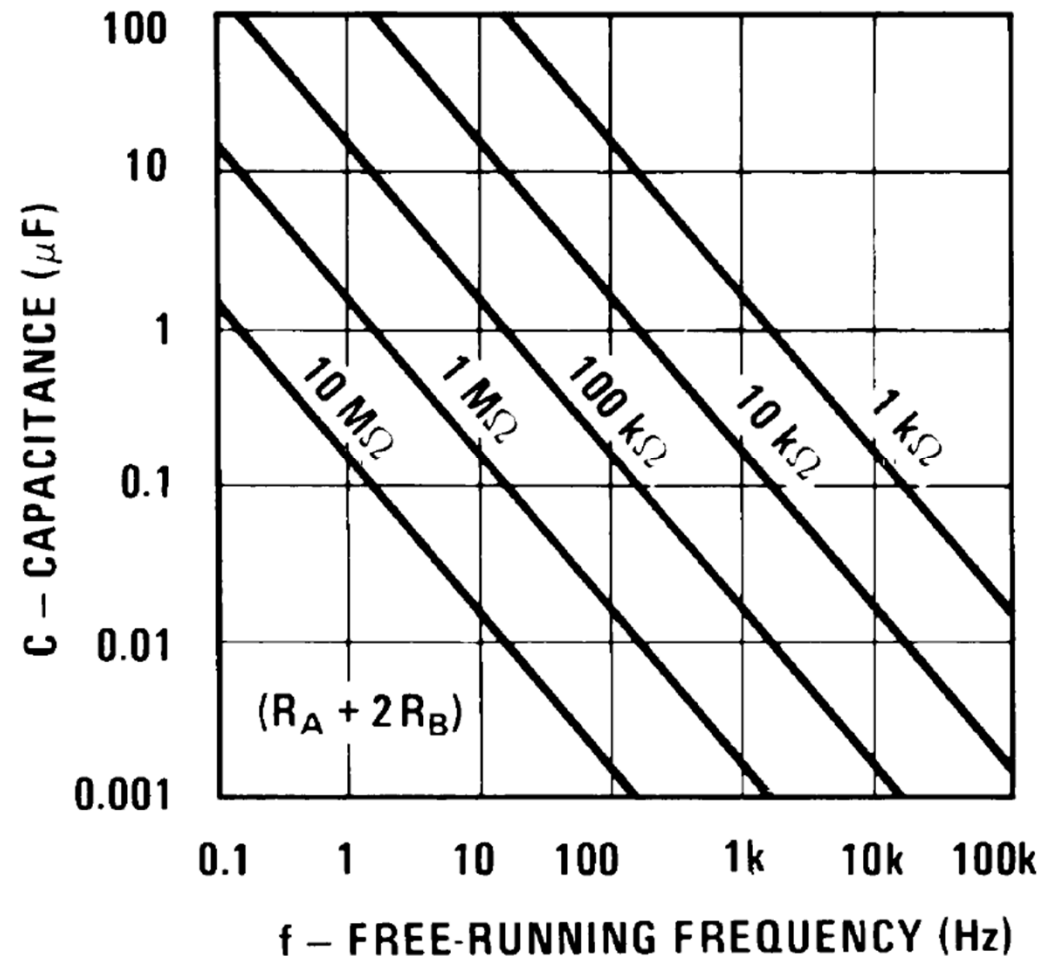
$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

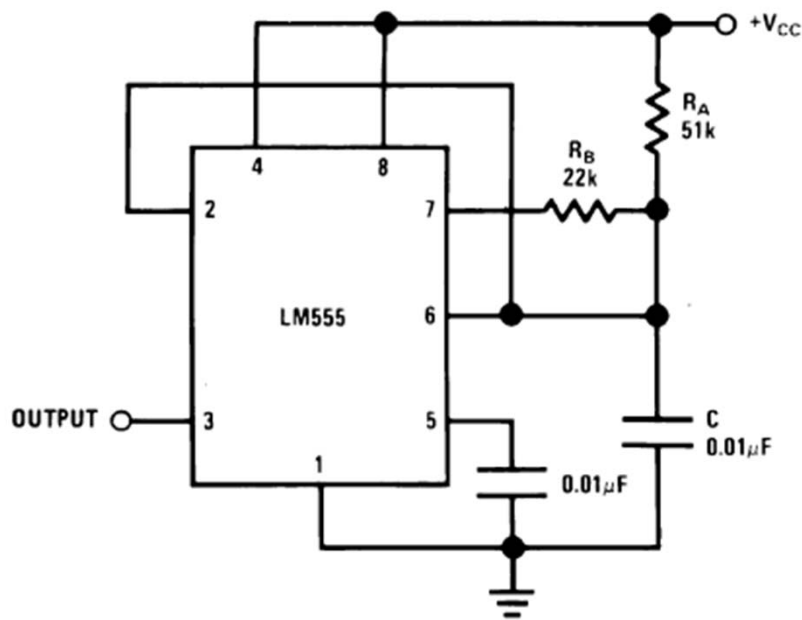
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$



Note: Max  $R_A + 2R_B$  is  $20M\Omega$

# 50% Duty Cycle Clock with 555



00785118

For a 50% duty cycle, the resistors  $R_A$  and  $R_B$  may be connected as in *Figure 14*. The time period for the output high is the same as previous,  $t_1 = 0.693 R_A C$ . For the output low it is  $t_2 =$

$$\left[ \frac{R_A R_B}{R_A + R_B} \right] C \ln \left[ \frac{R_B - 2R_A}{2R_B - R_A} \right]$$

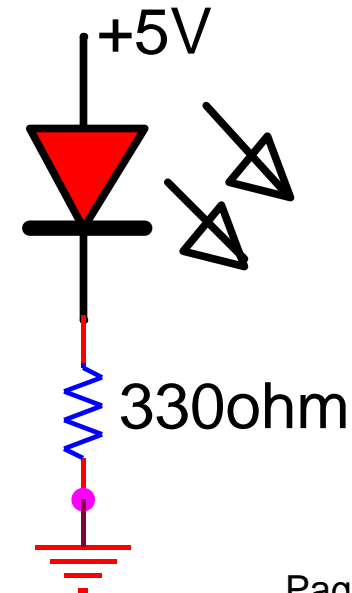
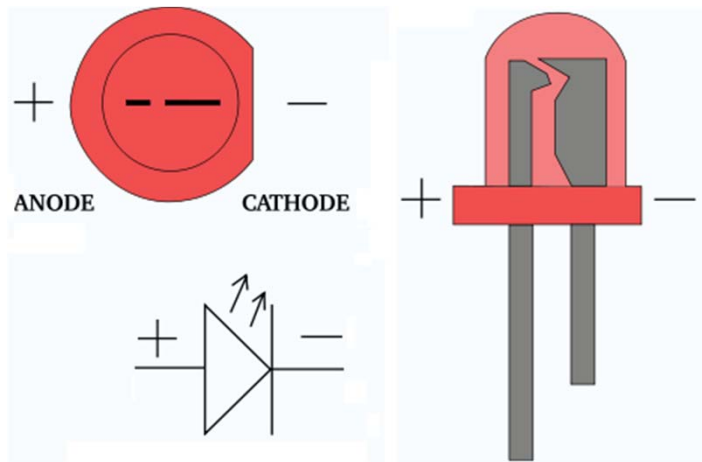
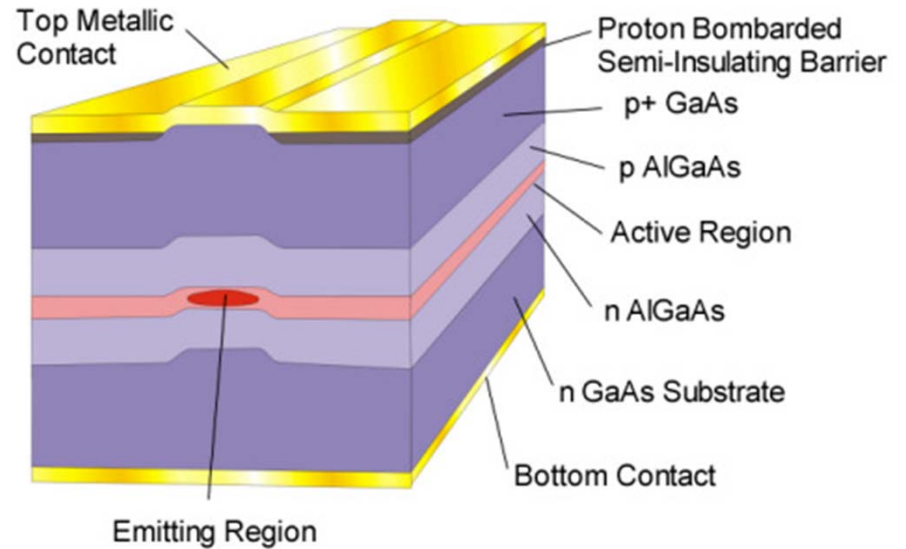
Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

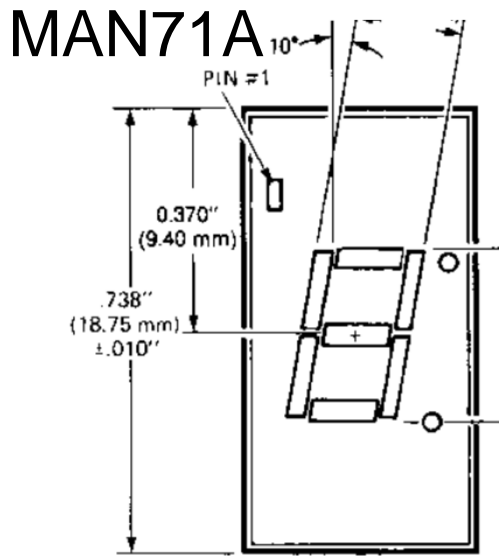
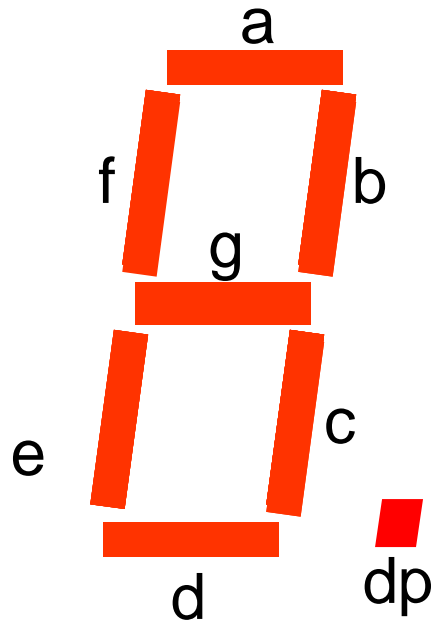
# Display Technologies-LED

## LED - Light Emitting Diode

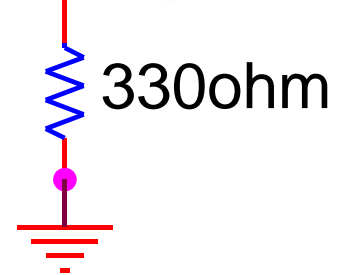
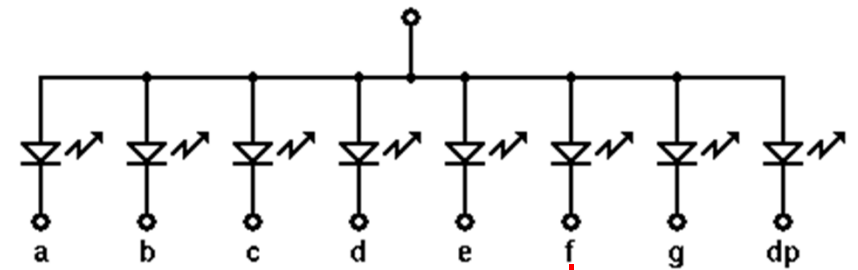
- Normally operates at  $\sim 10\text{mA}$
- Drops  $\sim 1.7\text{V}$
- Has typical Solid State Diode IV Characteristics
- Available in many different colors (Physics achievement!)



# 7-Segment LED Display



Connected to +5V  
COMMON ANODE



Pin No.	A MAN3410A, 3610A, 71A, 3810A
1	Cathode A
2	Cathode F
3	Common Anode
4	No Pin
5	No Pin
6	No Connection
7	Cathode E
8	Cathode D
9	Cathode D.P.
10	Cathode C
11	Cathode G
12	No Pin
13	Cathode B
14	Common Anode

# LED Display Devices

## MAN71A 7-Segment Display

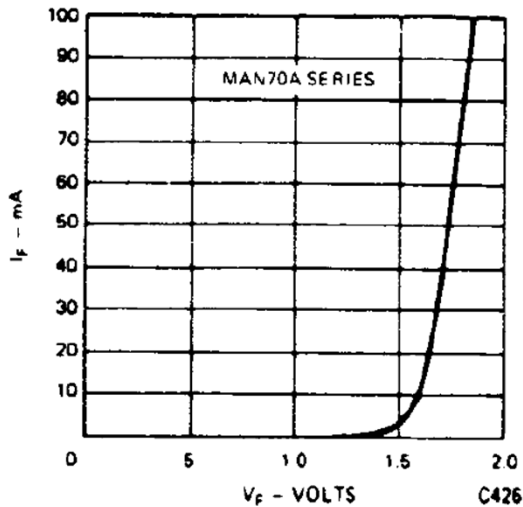


Fig. 6. Forward Current vs. Forward Voltage

<b>ELECTRO-OPTICAL CHARACTERISTICS</b> (25°C Free Air Temperature Unless Otherwise Specified) (Cont'd)					
	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
<b>MAN71A, 72A, 73A, 74A</b>					
Luminous Intensity, digit average (See Note 1 and 3)	125	350		$\mu\text{cd}$	$I_F = 10 \text{ mA}$
Peak emission wavelength		660		nm	
Spectral line half width		20		nm	
Forward voltage					
Segment			2.0	V	$I_F = 20 \text{ mA}$
Decimal point			2.0	V	$I_F = 20 \text{ mA}$
Dynamic resistance					
Segment		2		$\Omega$	$I_{pk} = 100 \text{ mA}$
Decimal point		2		$\Omega$	$I_{pk} = 100 \text{ mA}$
Capacitance					
Segment		35	80	pF	$V = 0$
Decimal point		35	80	pF	$V = 0$
Reverse current					
Segment			100	$\mu\text{A}$	$V_R = 5.0 \text{ V}$
Decimal point			100	$\mu\text{A}$	$V_R = 5.0 \text{ V}$
<b>MAN71A MAN72A MAN74A</b>					
Power dissipation at 25°C ambient				480 mW	
Derate linearly from 50°C				-6.9 mW/°C	
Storage and operating temperature				-40°C to +85°C	
Continuous forward current					
Total				240 mA	
Per segment				30 mA	
Decimal point				30 mA	
Reverse voltage					
Per segment				6.0 V	
Decimal point				6.0 V	
Soldering time at 260°C (See Notes 4 and 5)				5 sec.	

# BCD

Binary Coded Decimal maps a four bit binary code directly to decimal numbers.

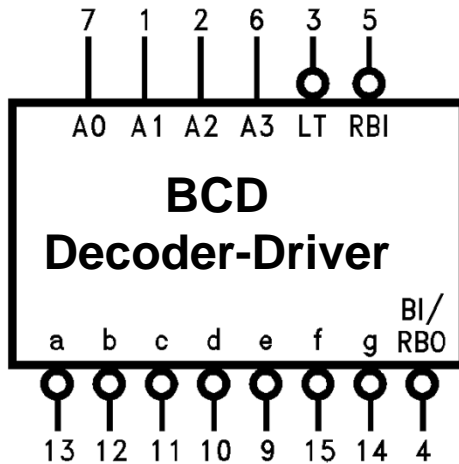
Great for using binary to provide the human interface, but is really inefficient binary “packing” so is rarely used internally in circuits.

Chips are available that perform the conversion binary  $\rightarrow$  BCD  $\rightarrow$  binary.

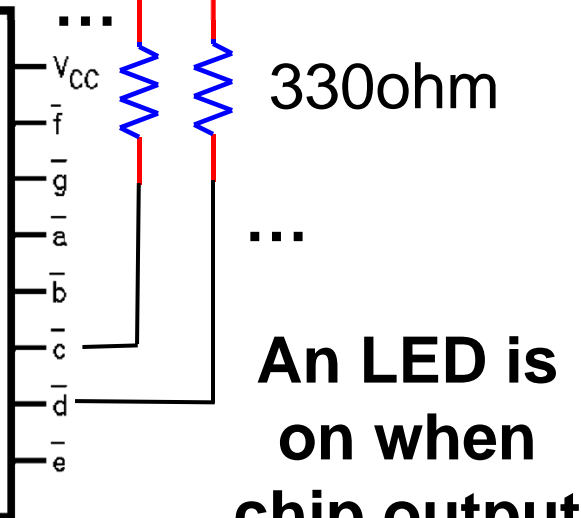
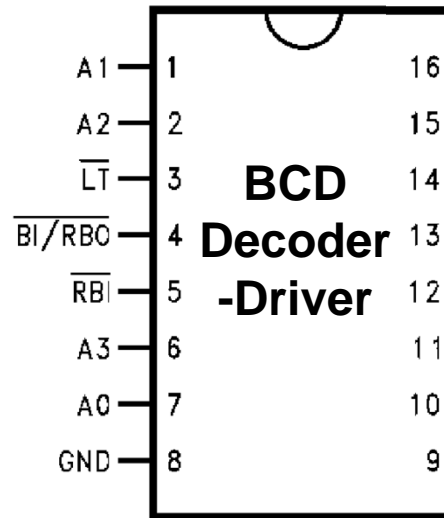
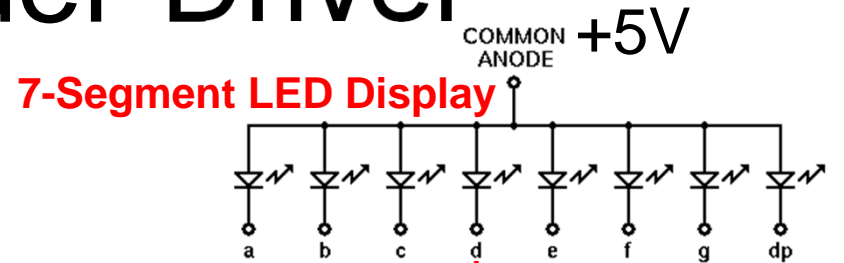
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Dec
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Undef
↓	↓	↓	↓	↓
1	1	1	1	Undef

# BCD Decoder-Driver

## Logic Symbol

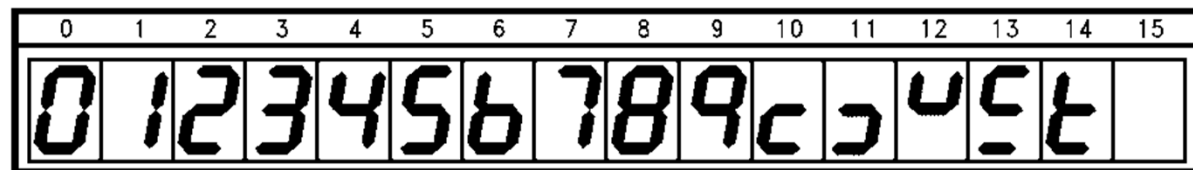


$V_{CC}$  = Pin 16  
GND = Pin 8



**An LED is on when chip output goes low.**

## Numerical Designations—Resultant Displays



**7-Segment LED Display**

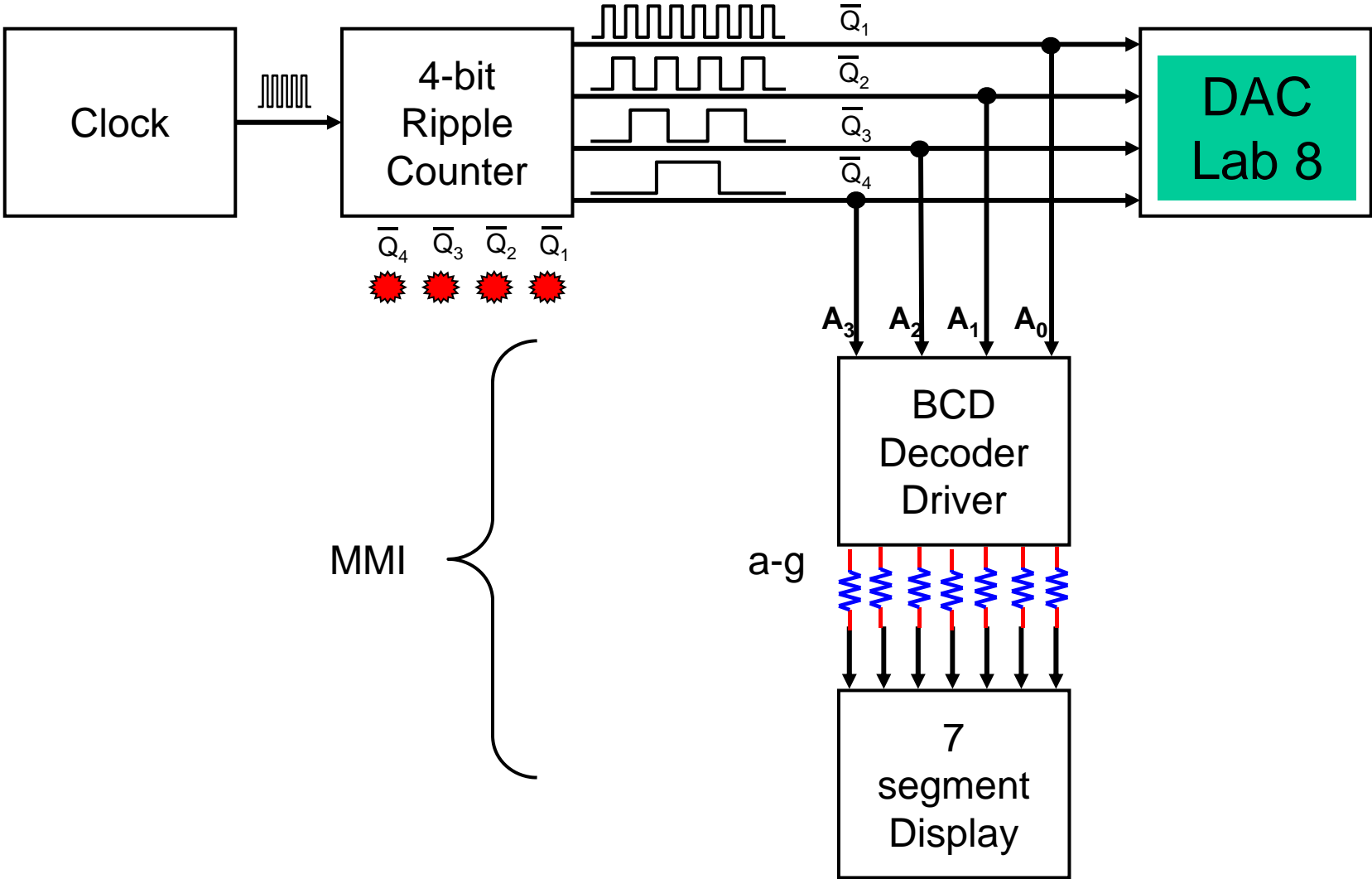


# Truth Table - BCD Decoder

DM74LS47

Truth Table															
Decimal or Function	Inputs							Outputs							Note
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A3	A2	A1	A0	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

# Lab 7: Ripple Counter with Display



Based with permission on lectures by John Getty