

Today

3/22/11 Lecture 9

Analog ↔ Digital Conversion

- **Sampled Data Acquisition Systems**
- **Discrete Sampling and Nyquist**
- **Digital to Analog Conversion**
- **Analog to Digital Conversion**

Homework

- **Study for Exam next week (in class 3/29/11)**
- **Covers everything up through Lecture 8 and Lab 7**

Reading

- **A/D converters (pages 612-641).**

Lab

- **Do DAC pre-lab before lab meeting.**
 - **Graded at start of lab!!!**
- **Sequential logic lab book due 3/25 at 10am.**

Analog → Digital → Analog

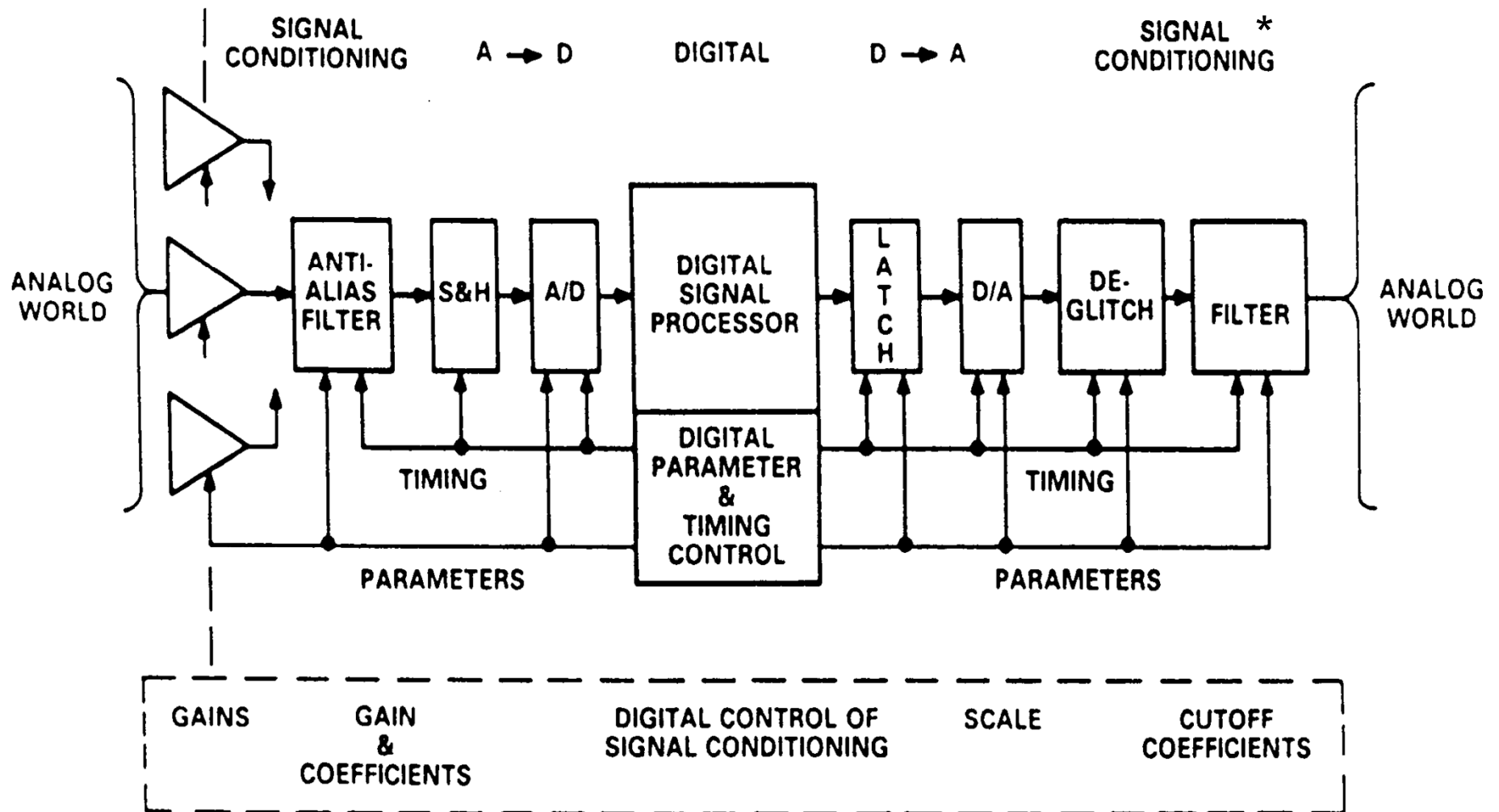
Why convert from analog to digital

- Digital transmission and storage of analog signals
 - Compression, Reliability, Error Correction
- Digital signal processing
 - Powerful algorithm, adaptable, ease of implementation

Why convert from digital to analog

- We live (see, hear, and feel) in an analog world
- Replay stored, transmitted, or processed data
 - Music, messages, movies
- Relay information from computers to humans
- Digital control of analog systems
- Convert virtual worlds to reality

Key Elements of a Sampled Signal Processing System



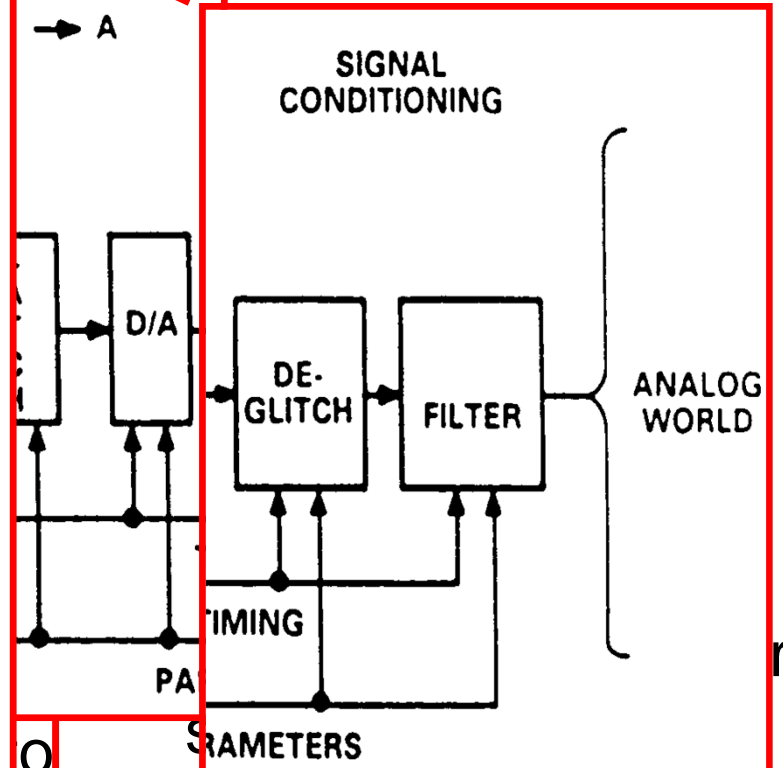
*ref: Analog Devices; Application Note AN-282

In many systems the signal is converted back into analog

Converts the analog signal

The final part of the process includes additional conditioning in the analog domain.

P is a



- Some D/As can produce in-band glitches that must be removed at this stage.
- Analog filtering can be used to compensate for the discrete nature of the D/A, improving overall system fidelity.

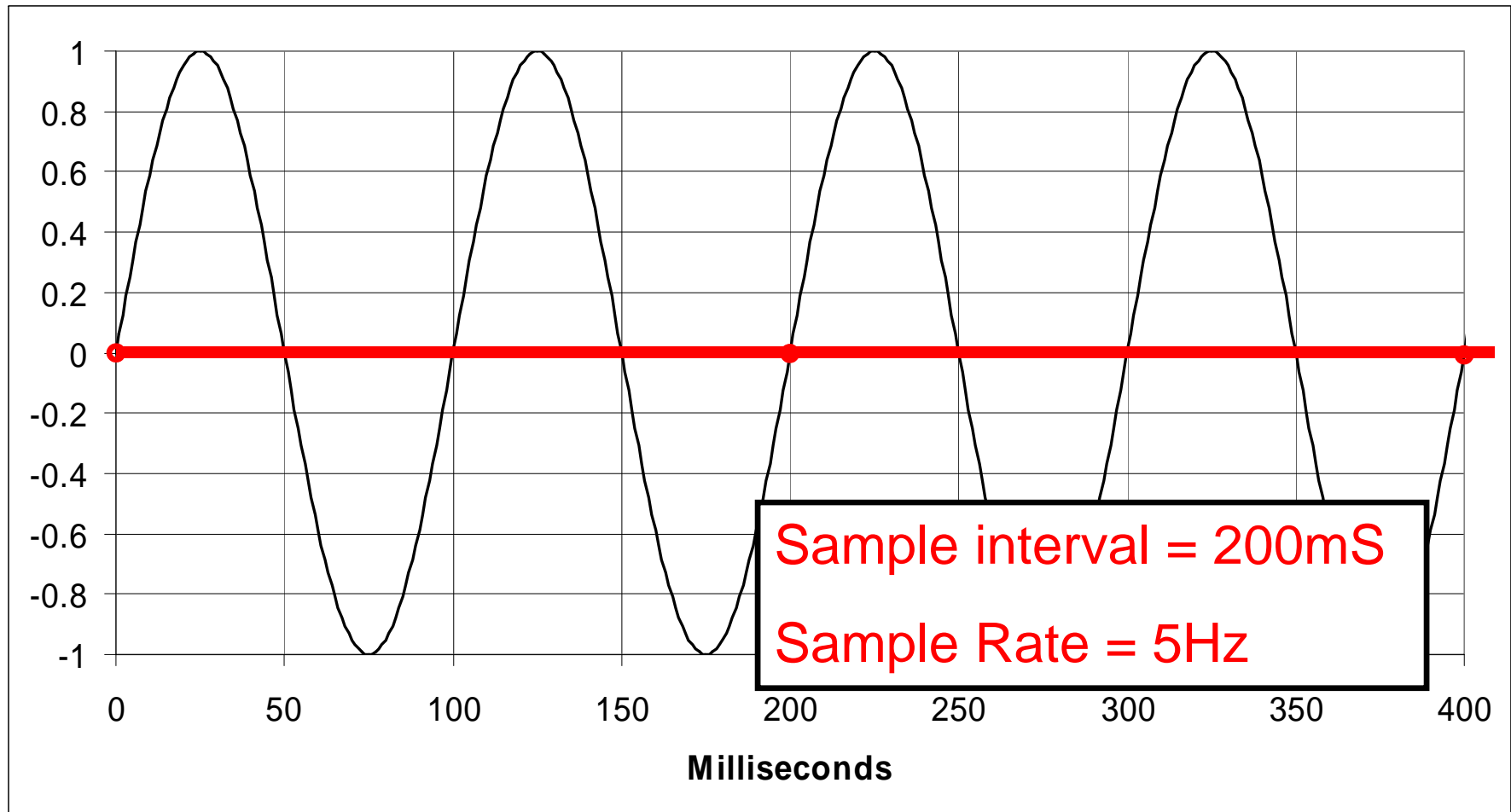
- Vector processors.
- Field programmable gate arrays (FPGA).

Some systems are made to faithfully reproduce (CD players) or improve (noise cancelling headphones) on the original analog input.

Analog Devices; Application Note AN-282

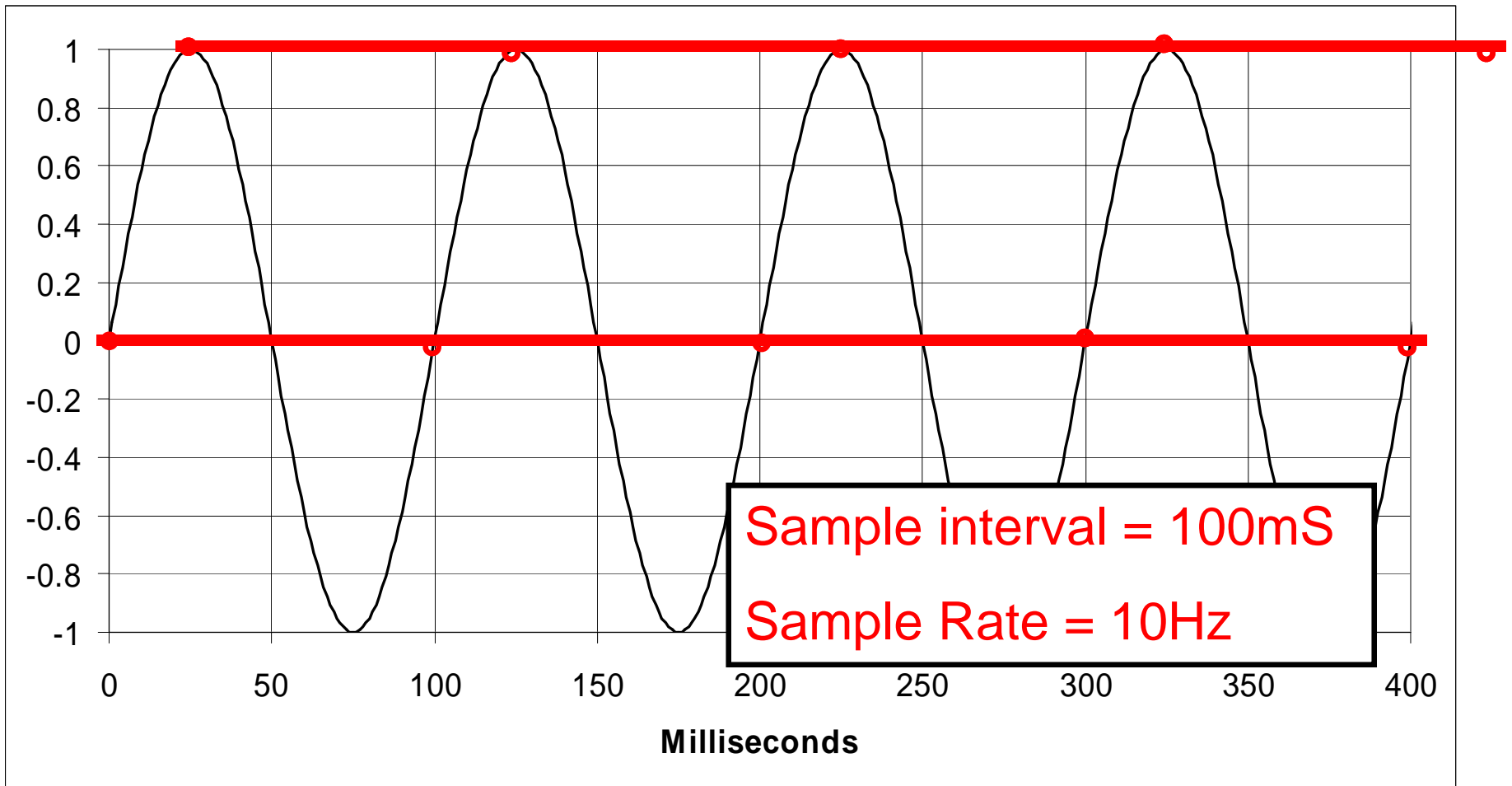
Discrete Sampling of 10 Hz Signal at 5Hz

$$f_{Signal} = 10Hz \quad f_{Sample} = 5Hz$$



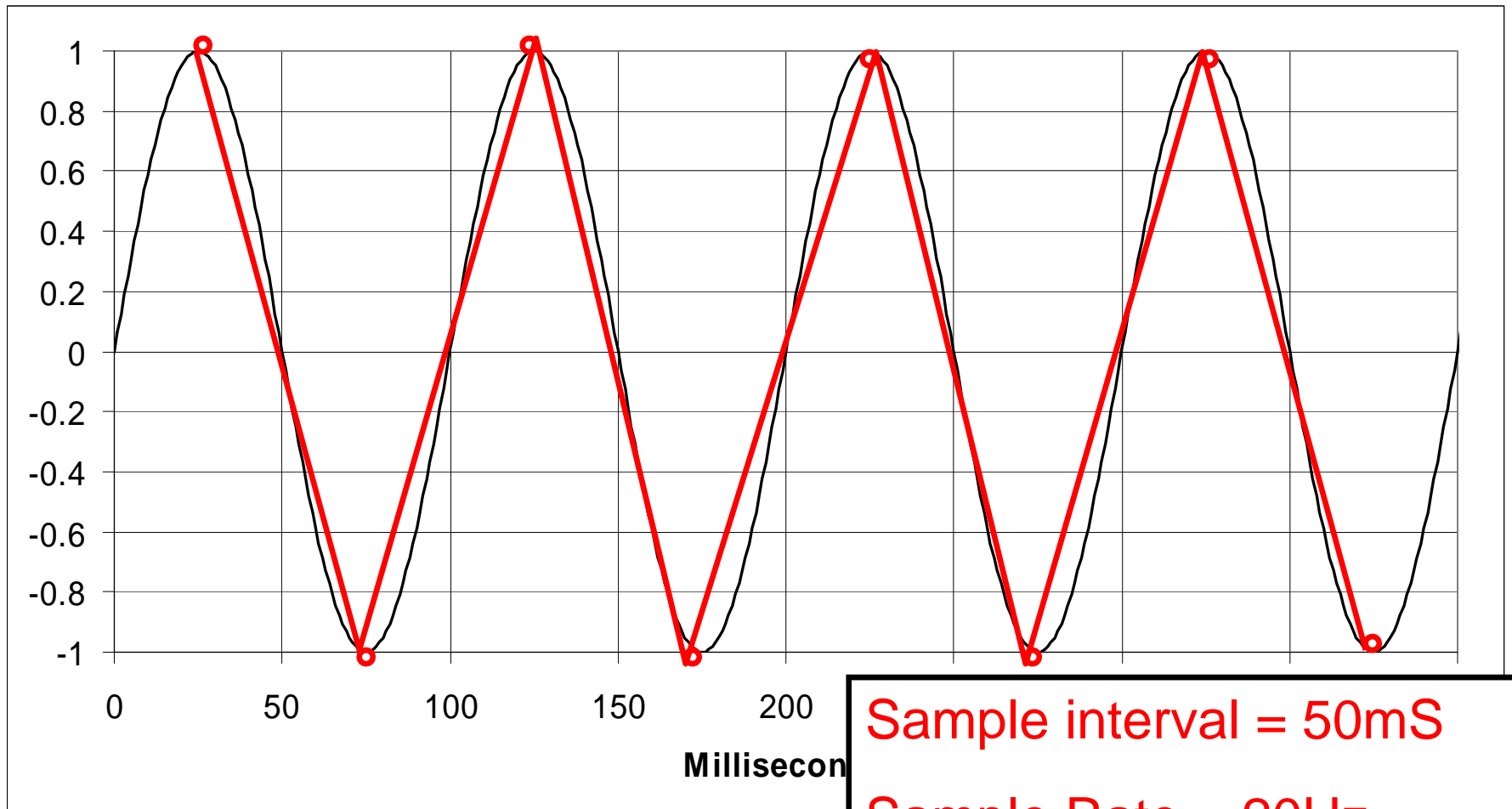
Discrete Sampling of 10Hz signal at 10Hz

$$f_{Signal} = 10Hz \quad f_{Sample} = 10Hz$$



Discrete Sampling at 20Hz

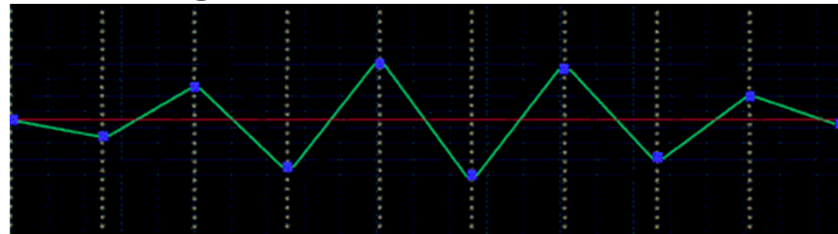
$$f_{Signal} = 10Hz \quad f_{Sample} = 20Hz$$



Nyquist Sampling Theorem

The sampling theorem states that for a limited bandwidth (band-limited) signal with maximum frequency f_{max} , the equally spaced sampling frequency f_{sample} must be **GREATER THAN** twice the maximum frequency of the signal, f_{max} , in order to uniquely reconstruct the signal without **aliasing**.

$$f_{sample} > 2f_{max}$$



$\Rightarrow 2f_{max}$ is called the **Nyquist sampling rate**.

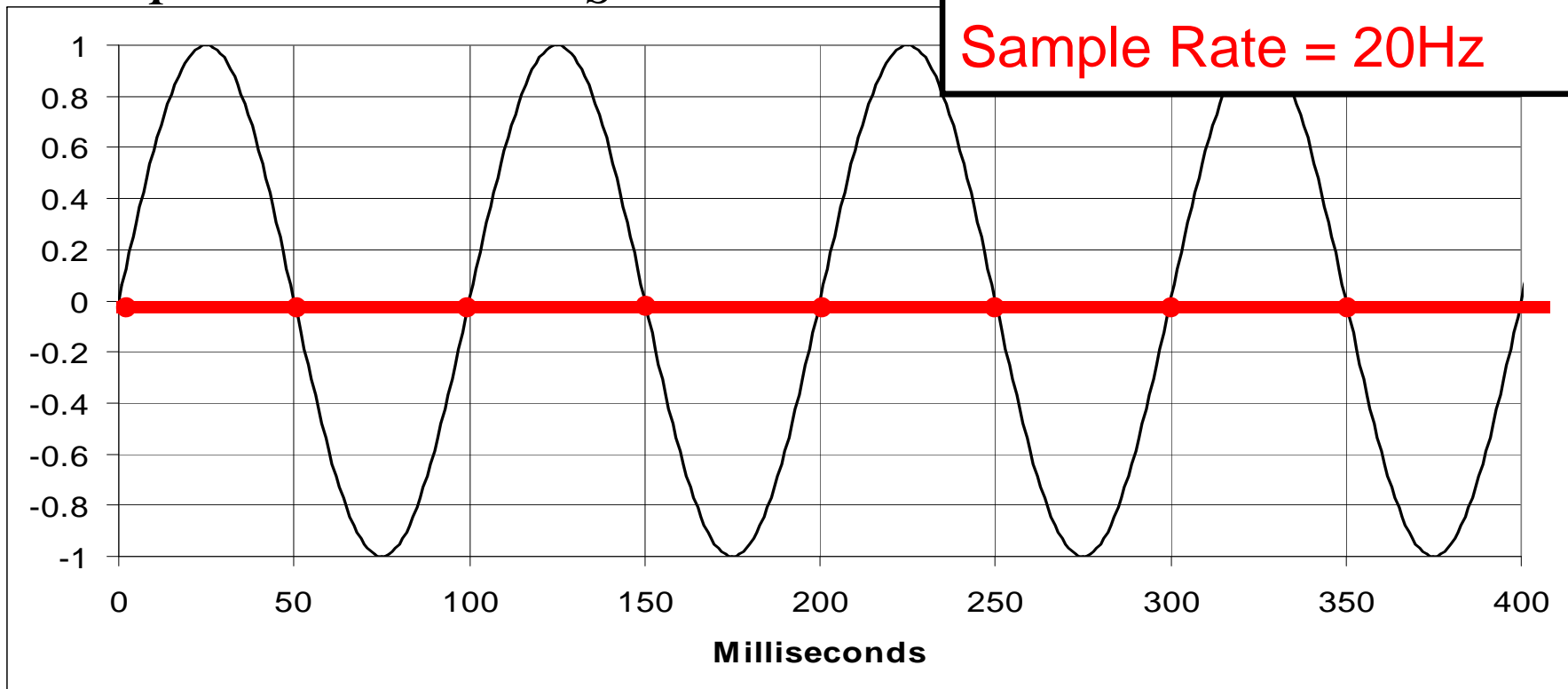
Half of the sampling rate of an A/D is sometimes called its **Nyquist frequency**, and is the max frequency that a A/D can record.

Discrete Sampling at $f_s = 2f_{max}$

$$f_F = 10\text{Hz} \quad f_s = 20\text{Hz}$$

Sample interval = 50mS

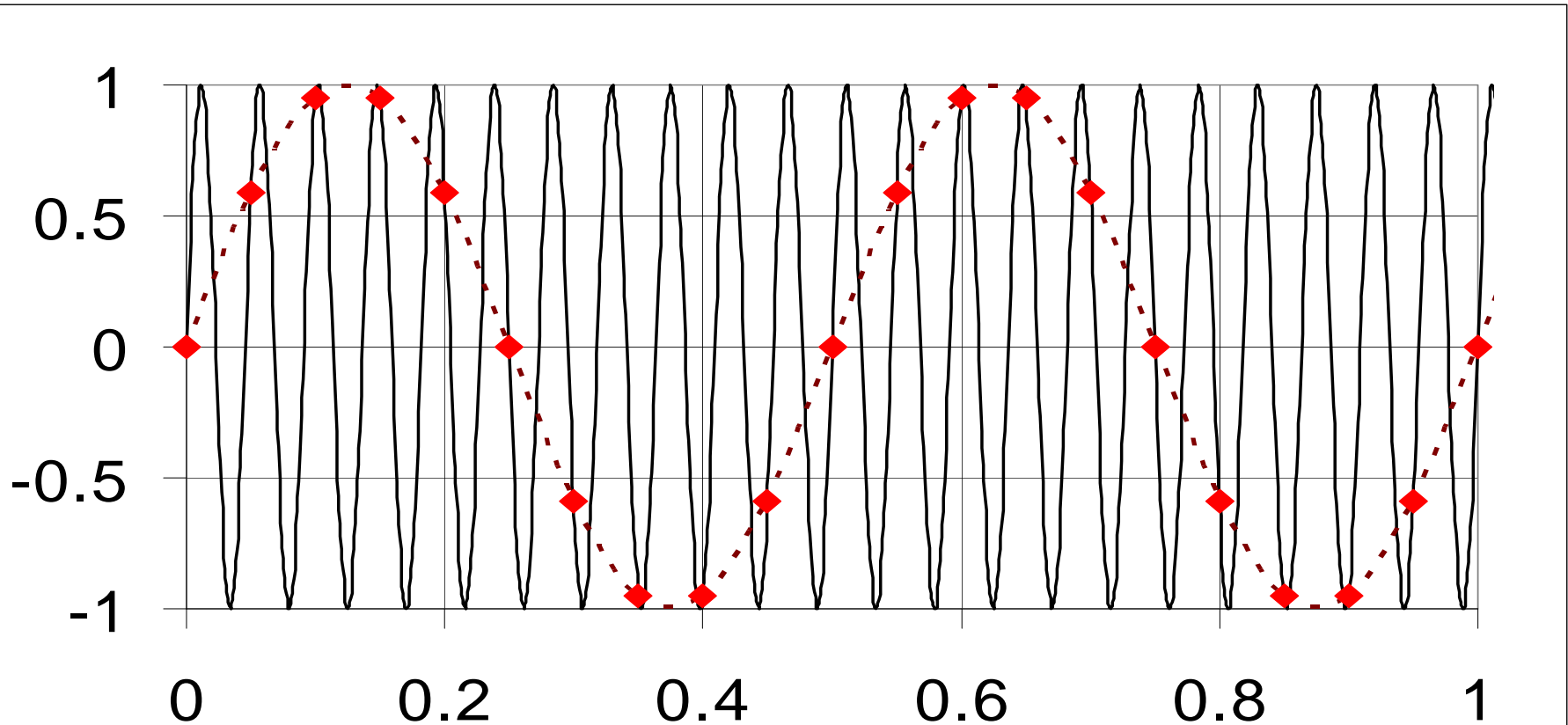
Sample Rate = 20Hz



$f_s = 2f_{max}$ is not sufficient,

Nyquist sampling requires $f_s > 2f_{max}$

Aliasing



Original Signal

$$f_{Sig} = 22Hz$$

Sample Freq.

$$f_{Samp} = 20Hz$$

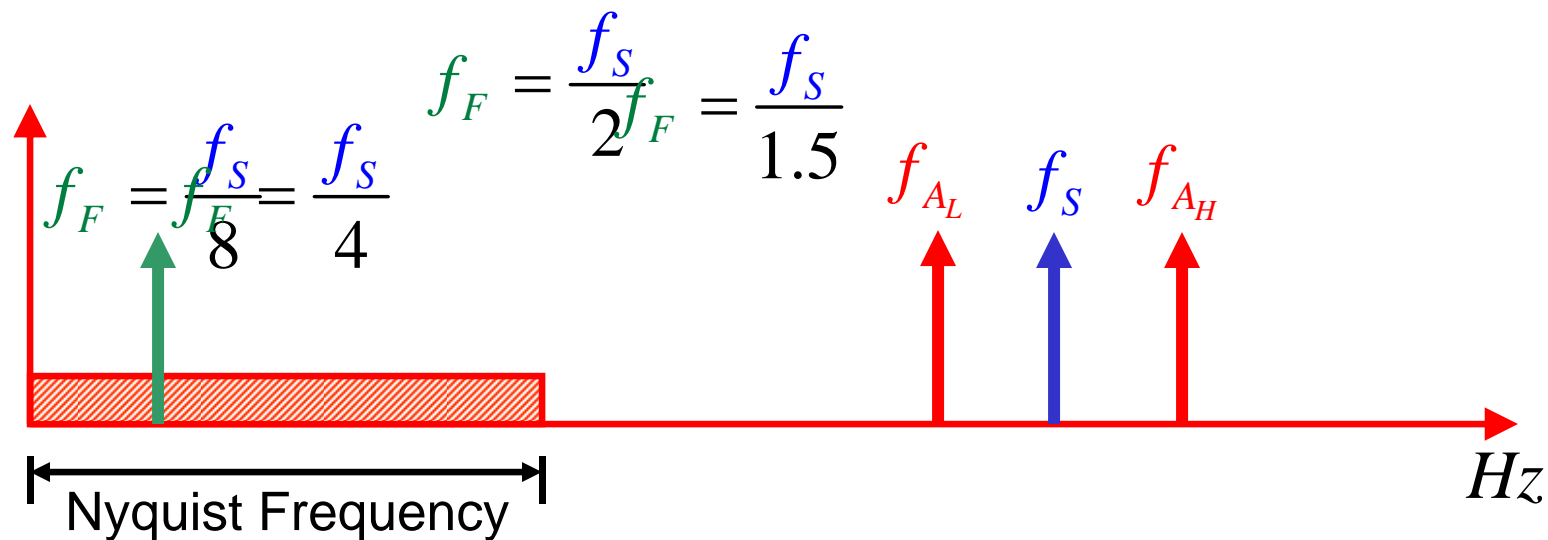
Sample Period

$$T_{Samp} = 50mS$$

Aliasing in the Frequency Domain

The frequency of aliased signals is the difference between and sum of the sampling frequency f_S and signal being sampled, f_F . These aliased signals repeat around each integer multiple of the sampling frequency.

$$f_{A_L} = f_S - f_F \quad \text{and} \quad f_{A_H} = f_S + f_F$$



If you low pass filtered at f_s , then you know only $f < f_s$ are real.

Digital to Analog Converter (DAC) Terminology

Number of Bits:

A DAC with n bits provides 2^n discrete output steps or *counts*. For example an 8 bit DAC has 256 possible output values.

Output Range:

Difference between the maximum and minimum output values.

Resolution:

Also known as the “step size”, represents the minimum change in output voltage. Typically equal to output range / $(2^n - 1)$

Dynamic Range:

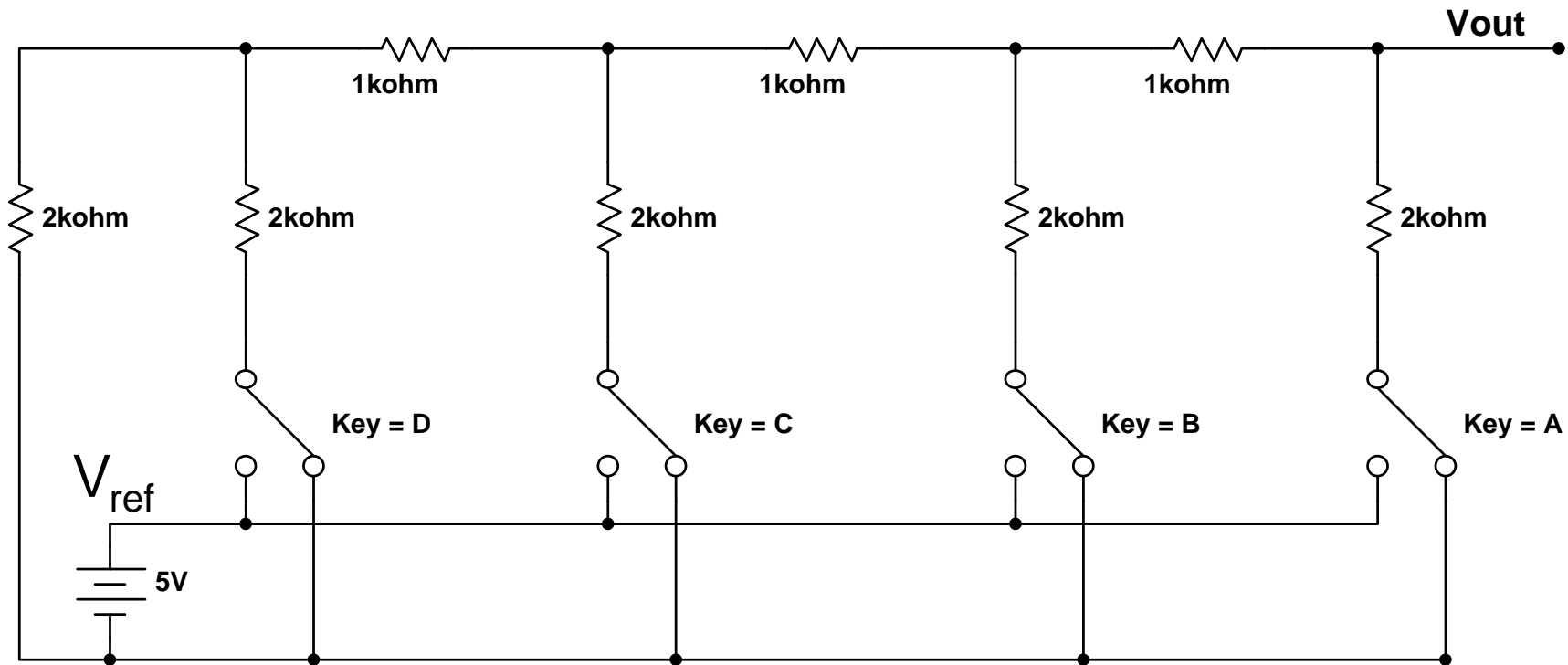
Output Range divided by Resolution or Noise Voltage. Would be $(2^n - 1)$ if the noise was less than step size of DAC.

In-Class Exercise

Assume a 10 bit DAC is set up to output a voltage from $-12V_{dc}$ to $+12V_{dc}$. Determine the resolution.



One Approach to DAC: R-2R Ladder Circuit

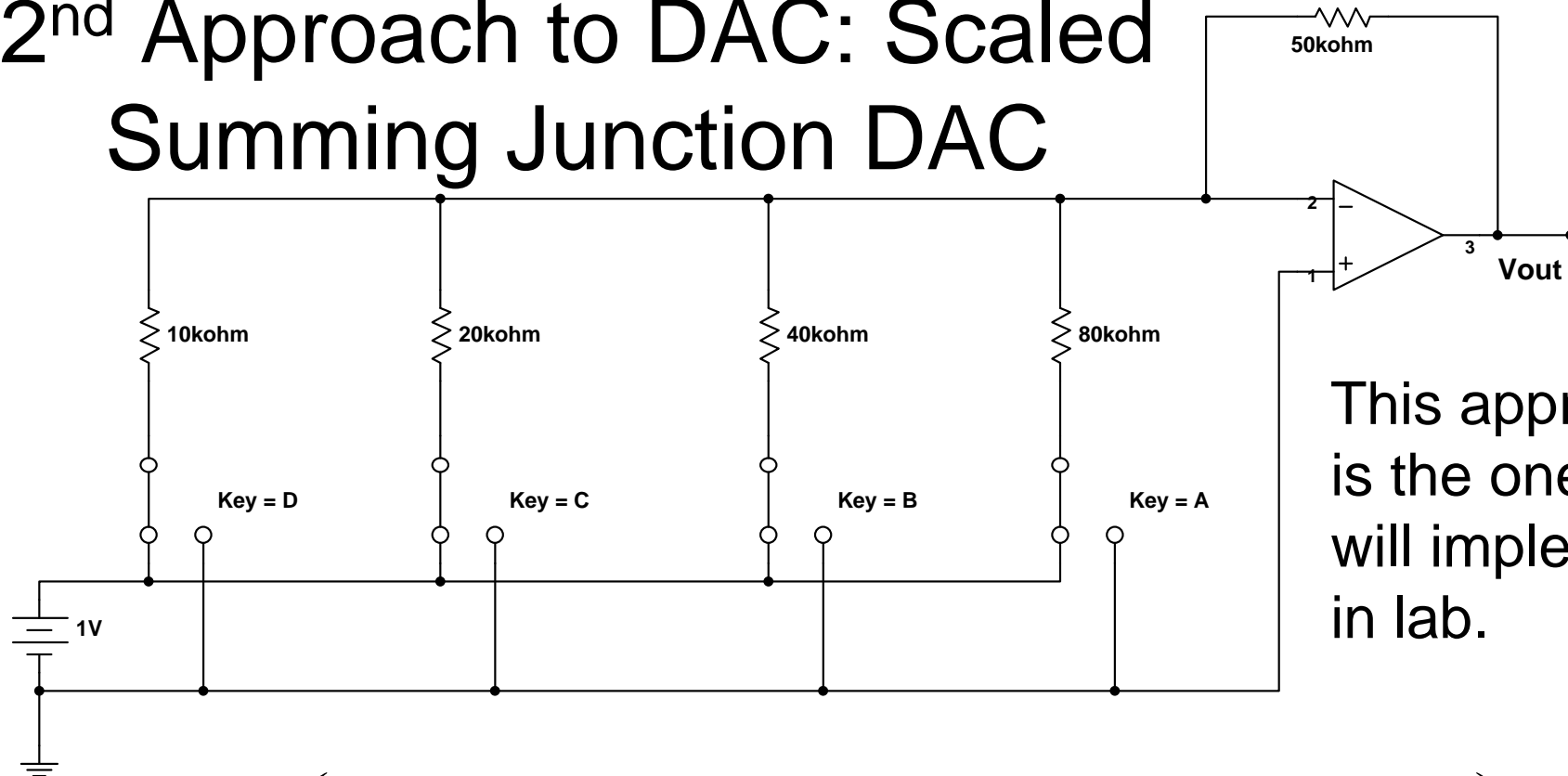


$$V_{out} = 5 \cdot \left(\frac{A}{2^1} + \frac{B}{2^2} + \frac{C}{2^3} + \frac{D}{2^4} \right) V$$

What is V_{max} ?

$$V_{max} = V_{ref} \cdot 15/16 = 4.69V \quad V_{min} = 0$$

2nd Approach to DAC: Scaled Summing Junction DAC



This approach is the one we will implement in lab.

$$V_{out} = -1V \cdot \left(\frac{A \cdot 50k\Omega}{80k\Omega} + \frac{B \cdot 50k\Omega}{40k\Omega} + \frac{C \cdot 50k\Omega}{20k\Omega} + \frac{D \cdot 50k\Omega}{10k\Omega} \right)$$

$$= -10 \cdot \left(\frac{A}{2^4} + \frac{B}{2^3} + \frac{C}{2^2} + \frac{D}{2^1} \right) V$$

What is Range?

$$V_{max} = 0, \quad V_{min} = -10V \cdot 15/16 = -4.69V$$

$$\text{Range} = 4.69V$$

Analog to Digital Converter (ADC) Terminology

Number of Bits:

An ADC with n bits divides the input range into 2^n discrete steps. For example, an 8 bit ADC can produce a total of 256 different output codes.

Full Scale Input Range

Difference between the minimum and maximum input voltage that can be measured.

Resolution:

Quantization, also known as the “step size”, is the change in input voltage represented by each count at the output. Often referred to as LSB (least significant bit)

Dynamic Range:

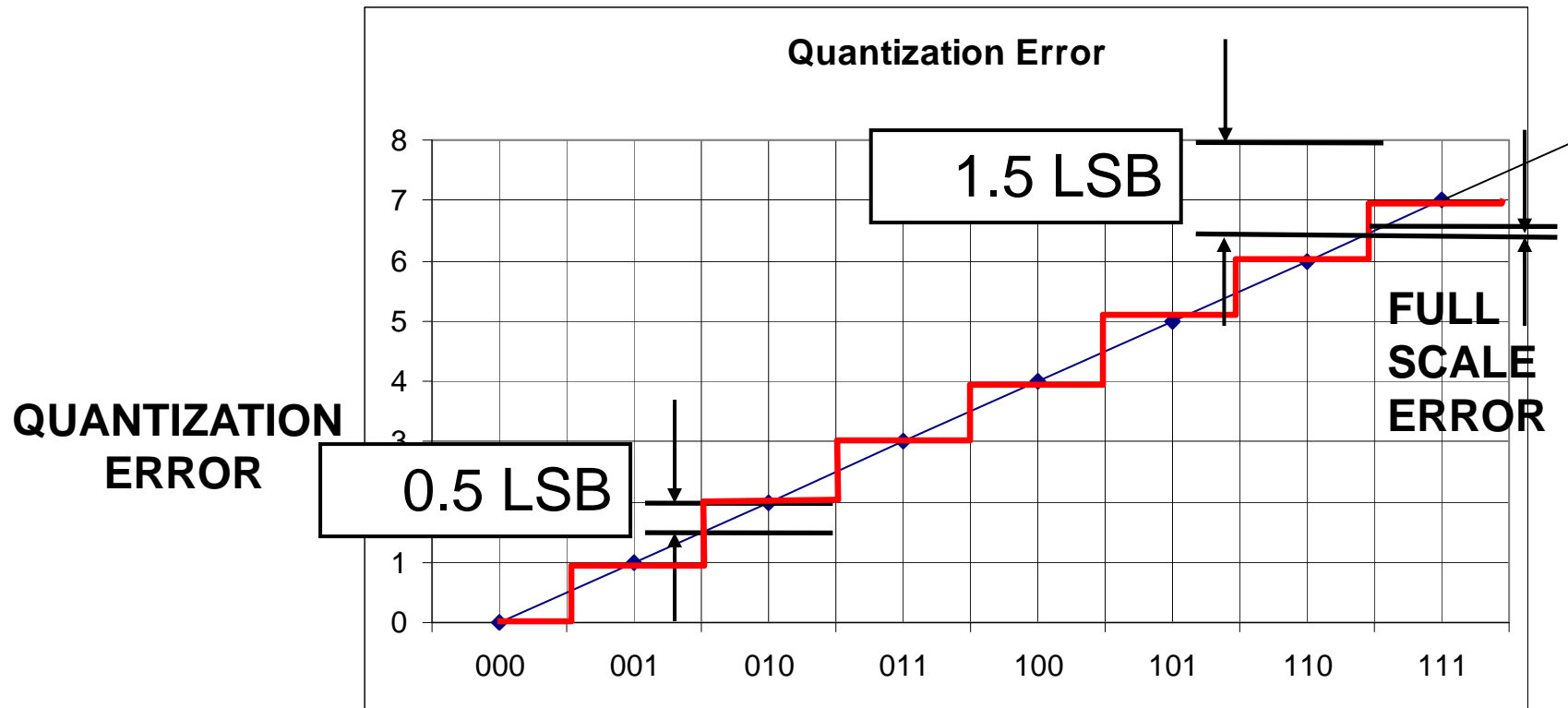
Input Range divided by resolution or noise. Typically equals $2^n - 1$, if noise is less than LSB.

ADC Accuracy

- **QUANTIZATION ERROR** Inherent accuracy ($\pm 1/2$ LSB, least significant bit)
- **INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from zero scale or negative full scale ($1/2$ LSB below the first code transition) through positive full scale ($1/2$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.
- **DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB. DNL is commonly measured at the rated clock frequency with a ramp input.
- **MISSING CODES** are output codes that are skipped or never appear at the ADC outputs. These codes cannot be reached by any input value.
- **OFFSET ERROR** is the difference between the ideal and actual LSB transition point.
- **FULL SCALE ERROR** is how far the last code transition is from the ideal 1.5 LSB below positive V_{ref} (V_{ref} is 2^n times step size)
- **GAIN ERROR** is number of LSB “gained” from conversion from lowest to highest output. It is a measure of the deviation of the ADC from linear (gain = 1) conversion.

See figure 9.44 in H&H page 615

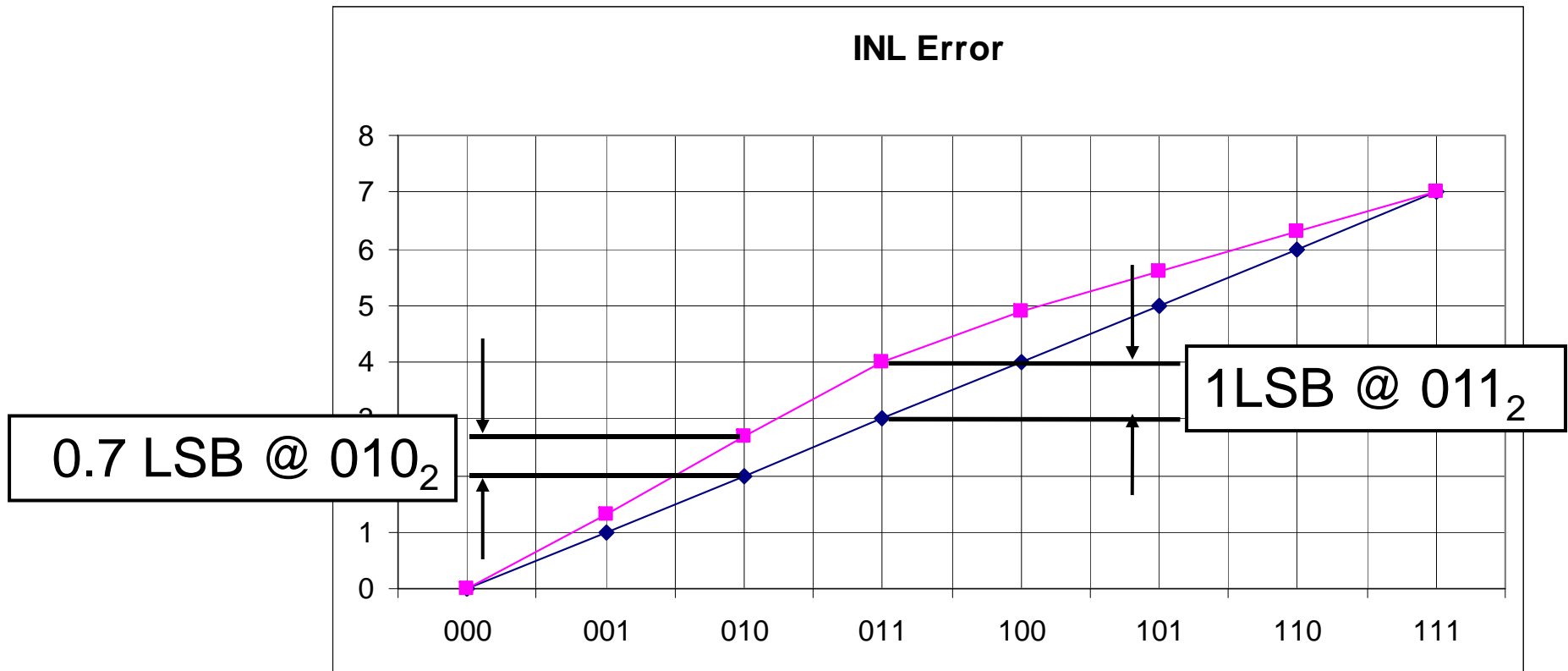
Ideal ADC: Quantization Error



-*Quantization error* is the inherent deviation of the output from a straight line.

-Note last transition is 1.5 LSB from V_{ref} (used to measure full scale error)

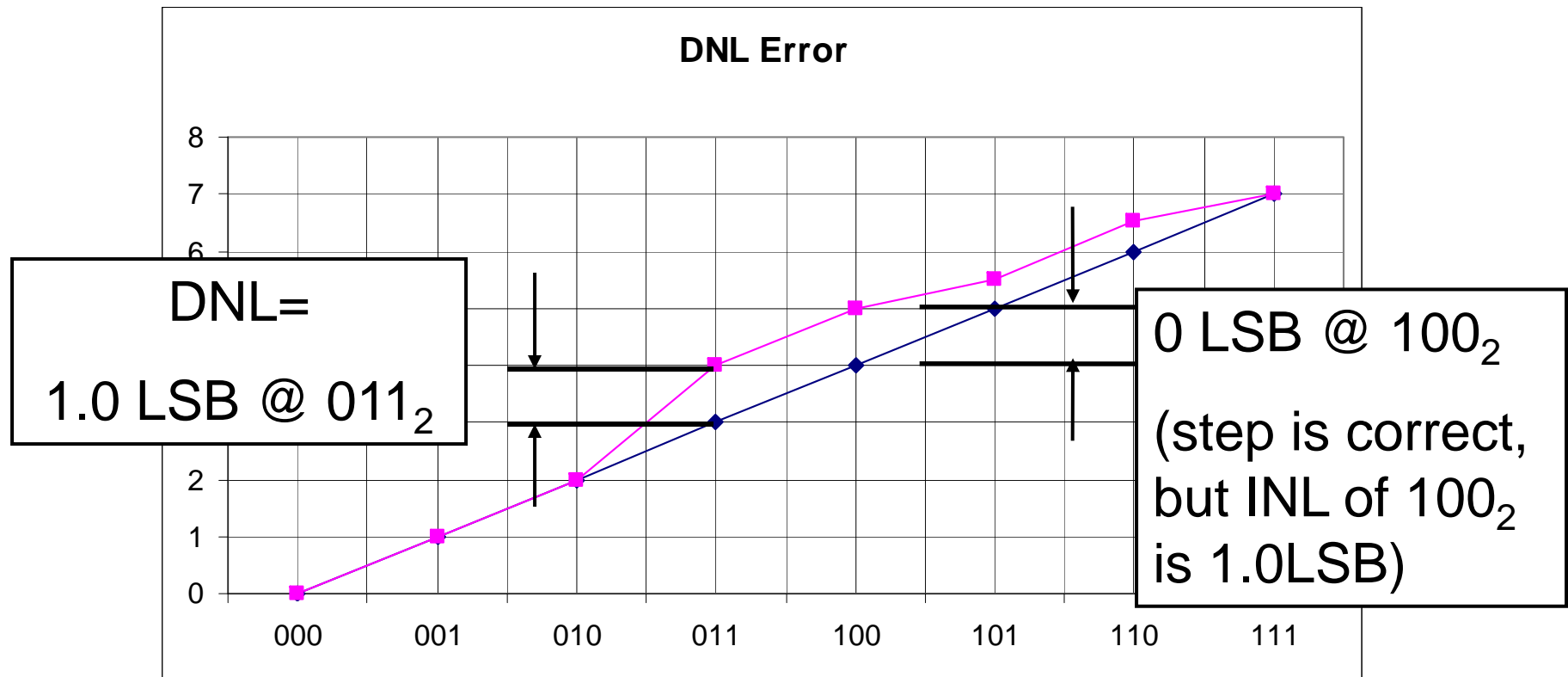
Sampled System Errors - INL



Integral Non-Linearity is the deviation of the output from a straight line.

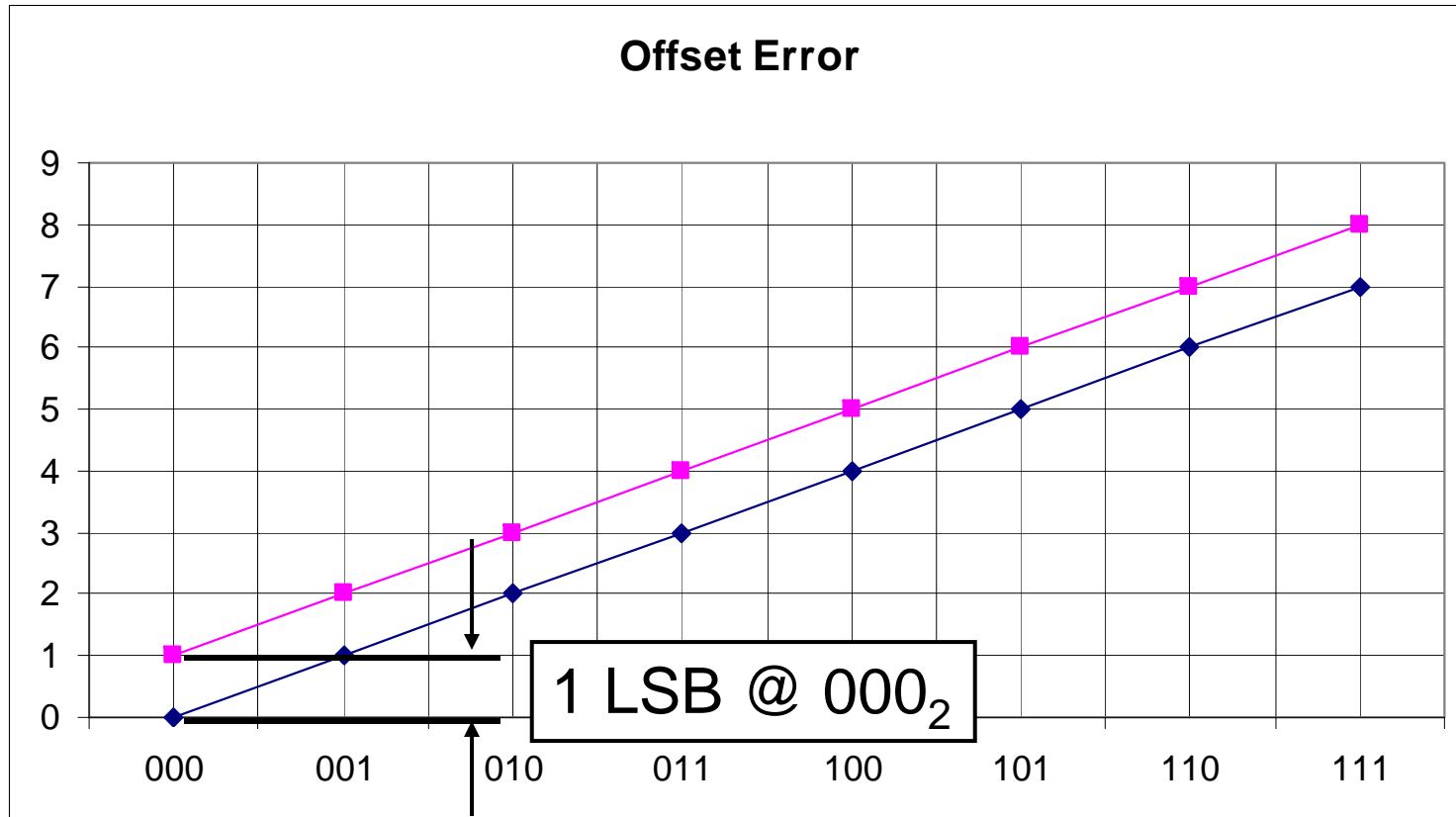
Can be measured at each code or stated as maximum for all codes.

Sampled System Errors - DNL



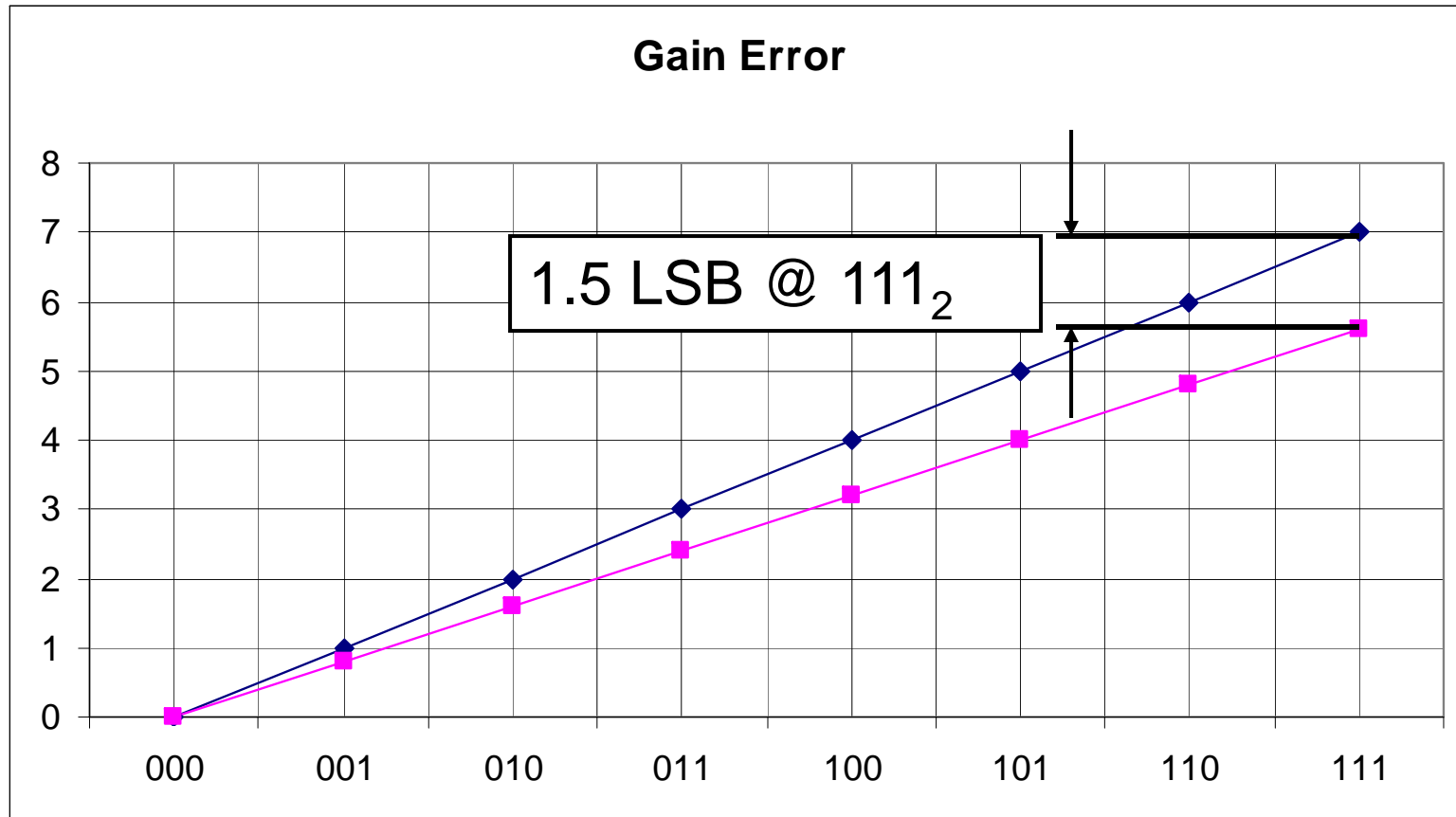
Differential Non-Linearity is the maximum difference between the expected stepsize (1 LSB) and that steps actually produced by the DAC.

Sampled System Errors - Offset



Offset Error is measured at 000₂.

Sampled System Errors - Gain

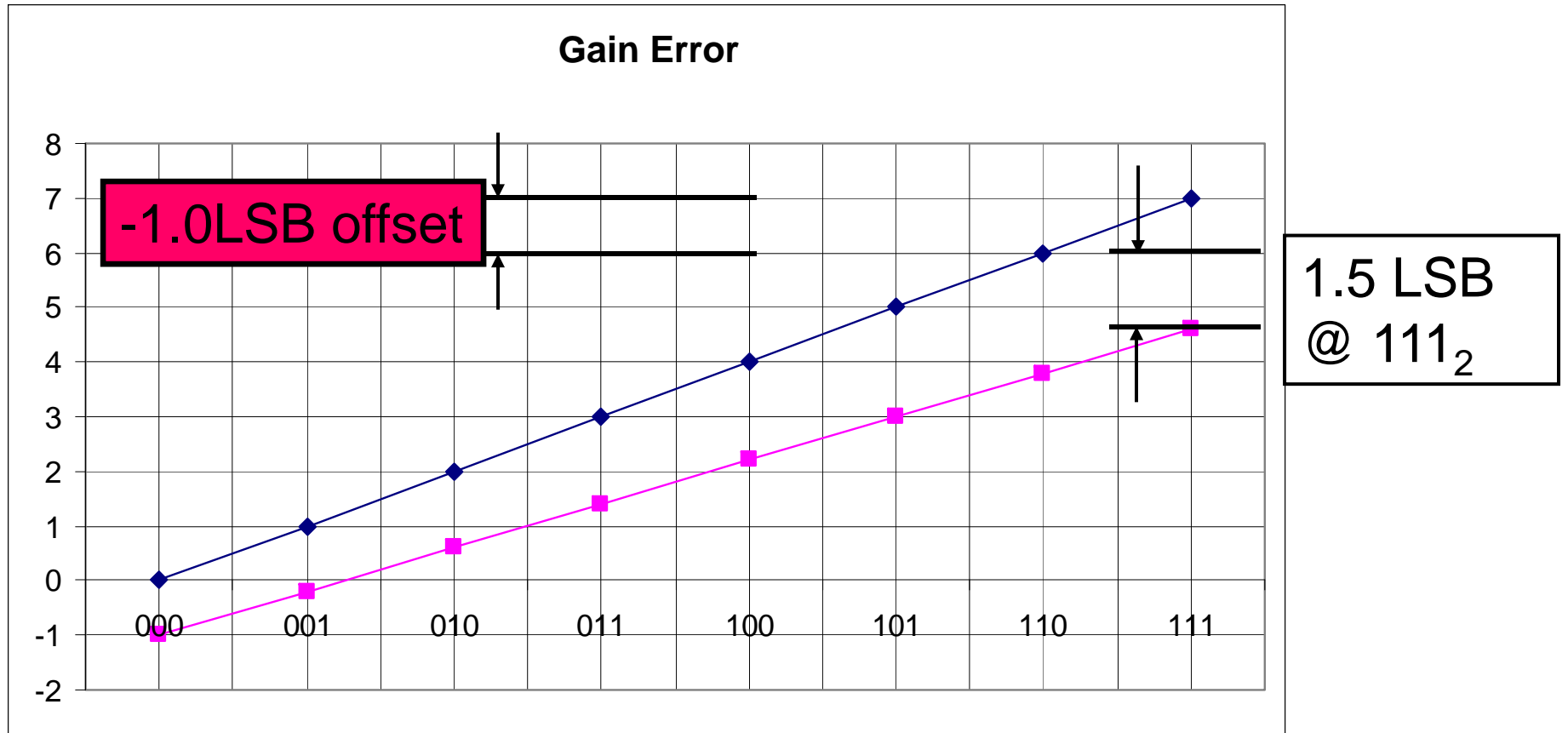


Gain Error is measured at 111_2 .

The offset error must be known to compute slope. ($y=mx+b$)

Gain Error is given in LSB over full scale.

Sampled System Errors - Gain



Gain Error is measured at 111_2 .

The offset error must be known to compute this value. ($y=mx+b$)

References

1. Paul Horowitz and Winfield Hill (1989). "The Art of Electronics," 2nd Ed., Cambridge
2. Analog Devices, "Fundamentals of Sampled Data Systems", accessed MAR 2008
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3. "EfunDa, Engineering Fundamentals" web site; accessed MAR 2008
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4. National Semiconductor: accessed MAR 2008
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