

OUTLINE

## COURSE UP TO EXAM 1:

- CURRENT, VOLTAGE, RESISTANCE AND OHM'S LAW
- TOOLS FOR CIRCUIT ANALYSIS
  - KIRCHHOFF'S LAWS (KVL, KCL)
  - SERIES & PARALLEL, VOLTAGE & CURRENT DIVISION
  - NODE VOLTAGE ANALYSIS
  - THÉVENIN & NORTON EQUIVALENTS

## TODAY'S LECTURE:

- SEMICONDUCTORS & P-N JUNCTIONS (CH. 40) — VERY BRIEF!
  - DIODES (CH. 41)
  - TRANSISTORS (CH. 42)
- } WE WILL FOCUS ON ELEMENTARY BEHAVIOR — LESS DETAIL THAN FORSSER.

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ANNOUNCEMENTS:

- HEADPHONE AMPLIFIER IS LAB # 9 & 11.

YOU HAVE 2 OPTIONS:

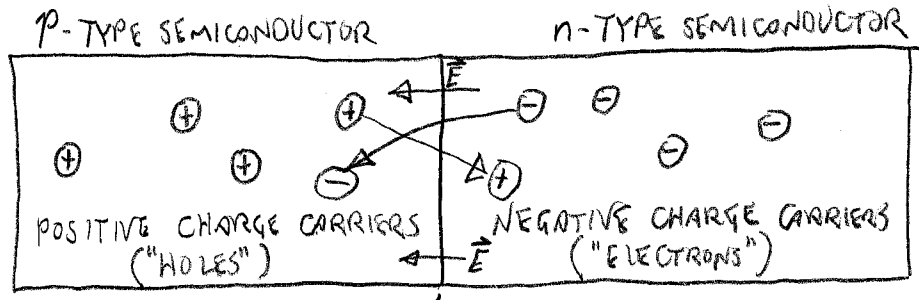
① BREADBOARD THE CIRCUIT AS USUAL

② SOLDER A PERMANENT CIRCUIT TO KEEP (COST \$15-20)

WHO WANTS TO BUY AN AMP KIT?

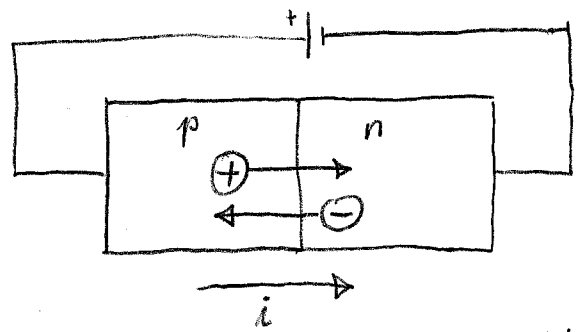
# P-N JUNCTION AND THE PHYSICS OF DIODES

Si (OR Ge) IS "DOPED" WITH IMPURITIES THAT PROVIDE CHARGE CARRIERS, ALLOWING IT TO CONDUCT.



DIFFUSION ACROSS PN JUNCTION SETS UP ELECTRIC FIELD  $\vec{E}$ .

## FORWARD BIAS:

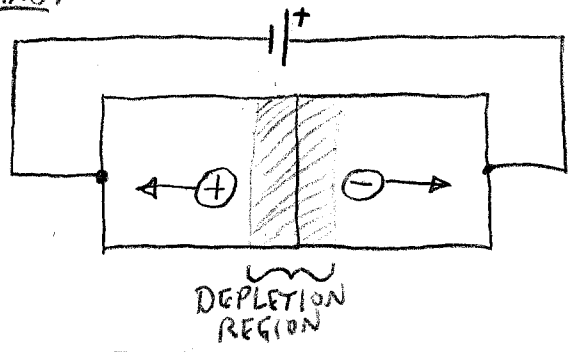


- ELECTRONS & HOLES CARRY THE CURRENT ACROSS THE JUNCTION.
- BOTH KINDS OF CARRIERS CAN PROPAGATE INTO THE OPPOSITE SIDE.

• A MINIMUM TURN-ON VOLTAGE  $V_T$  IS REQUIRED TO OVERCOME THE E-FIELD DUE TO DIFFUSION.

$$V_T \approx \begin{cases} 0.6 \text{ V} & (\text{Si}) \\ 0.3 \text{ V} & (\text{Ge}) \end{cases}$$

## REVERSE BIAS:



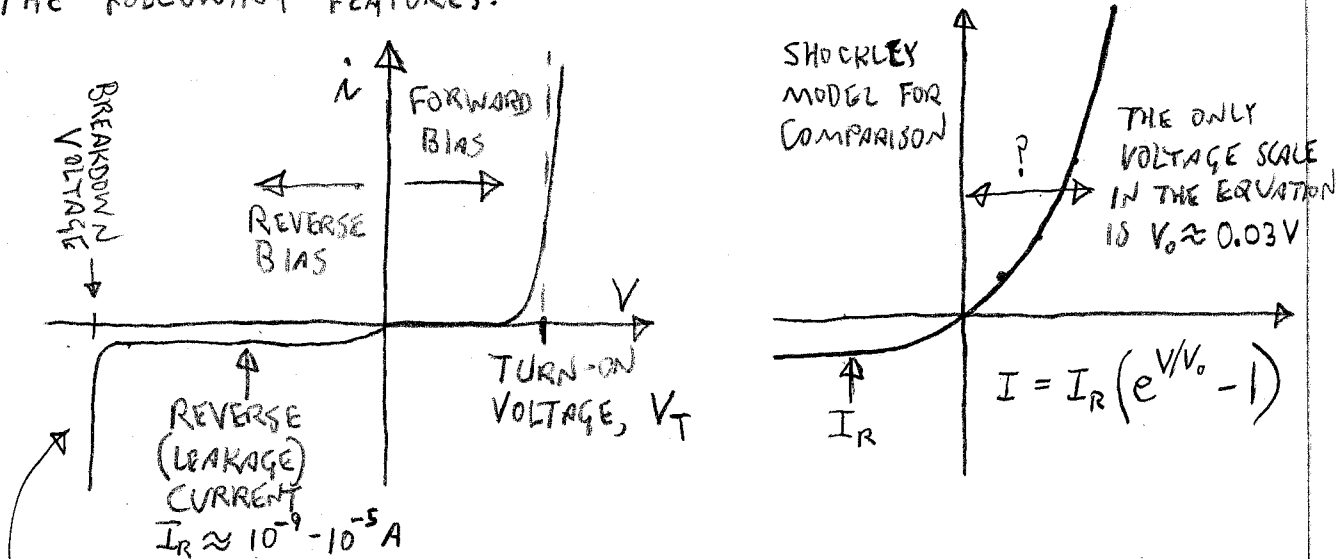
- BOTH ELECTRONS & HOLES MOVE AWAY FROM THE JUNCTION
- NO CHARGE CARRIERS, THEREFORE NO CURRENT.

THE p-n JUNCTION IS A DIODE, ALLOWING CURRENT TO FLOW ONLY ONE WAY.

# DIODE BEHAVIOR

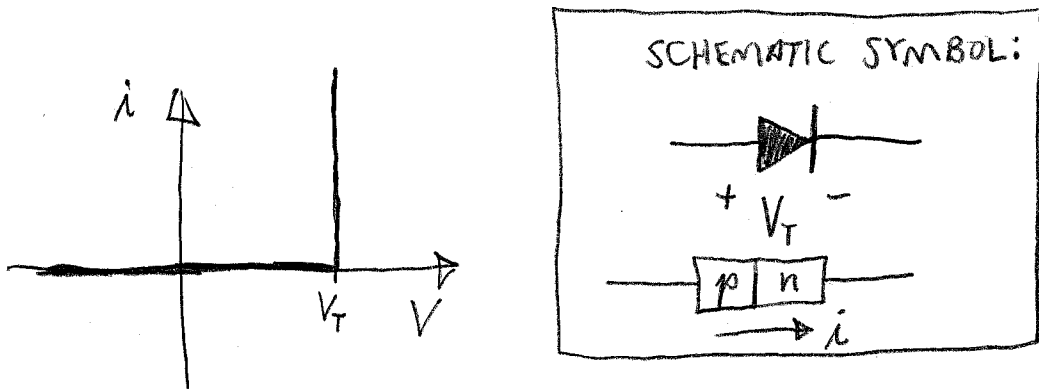
FAISSLER (CHS. 40-41) DESCRIBES DIODE BEHAVIOR USING THE SHOCKLEY EQUATION (EQS. 40-7 AND 41-1). THE ADVANTAGE OF THIS MODEL IS THAT IT'S EASY TO DERIVE FROM A SIMPLIFIED THEORY OF THE PN JUNCTION. UNFORTUNATELY IT DOESN'T ACCURATELY PREDICT THE TURN-ON VOLTAGE AND IS NOT VERY USEFUL FOR CIRCUIT ANALYSIS.

A MORE REALISTIC MODEL OF THE DIODE WOULD INCORPORATE THE FOLLOWING FEATURES:



BREAKDOWN IS USUALLY UNDESIRABLE (AND DESTRUCTIVE), EXCEPT IN ZENER DIODES, WHICH ARE ENGINEERED FOR NON-DESTRUCTIVE BREAKDOWN AT AN EXACT VOLTAGE.

WE WILL ADOPT THE FOLLOWING SIMPLIFIED MODEL FOR CIRCUIT ANALYSIS:



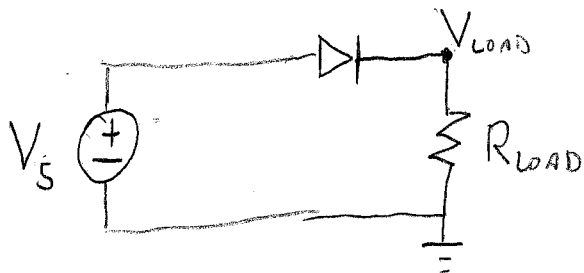
WHEN  $V < V_T$ , THE DIODE ACTS LIKE AN OPEN CIRCUIT  $\text{---} \text{---}$

WHEN  $V = V_T$ , THE DIODE MAY HAVE ANY POSITIVE CURRENT, AND ACTS LIKE A VOLTAGE SOURCE:



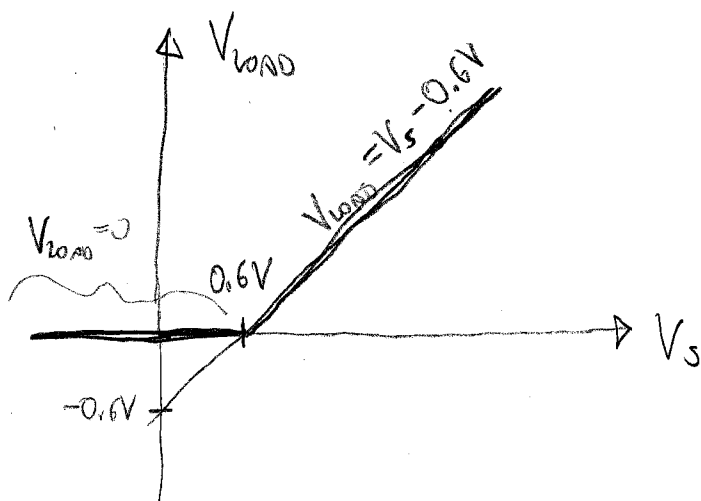
EXAMPLE

HALF-WAVE RECTIFIER



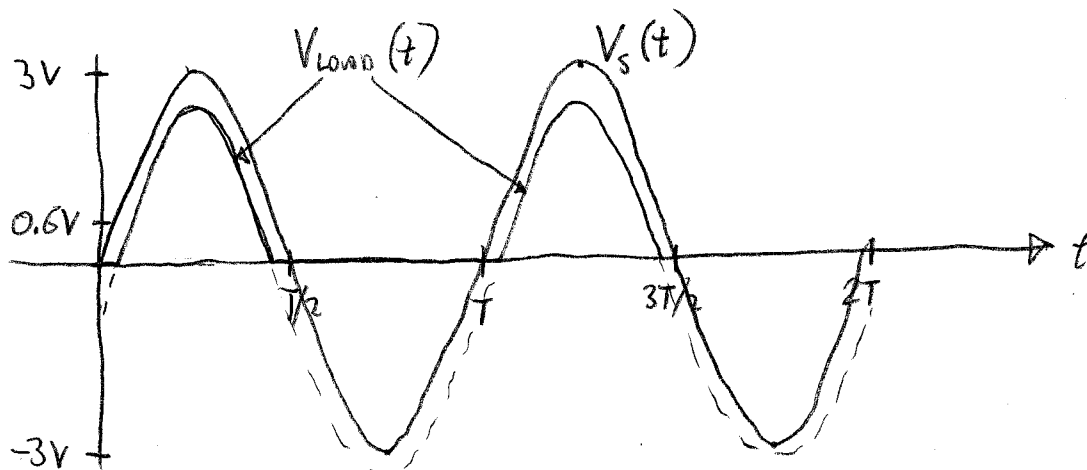
SI DIODE,  $V_s = 0.6V$

(a) PLOT  $V_{LOAD}$  AS A FUNCTION OF  $V_s$



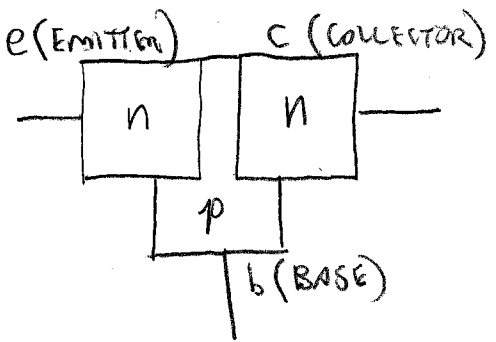
(b) SUPPOSE  $V_s = 3V \cdot \sin(2\pi t/T)$ .

SKETCH  $V_s(t)$  AND  $V_{LOAD}(t)$  ON THE SAME AXES.

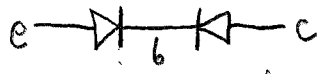


# TRANSISTORS

WE'LL ONLY CONSIDER BIPOLAR JUNCTION TRANSISTORS (BJTs), BUT VARIOUS KINDS OF FIELD EFFECT TRANSISTORS (FETs) HAVE LARGELY REPLACED BJTs IN MOST APPLICATIONS.



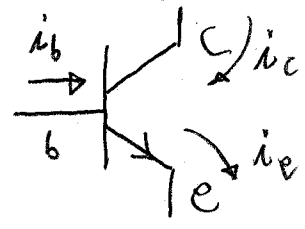
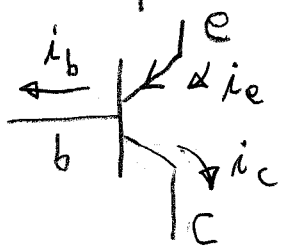
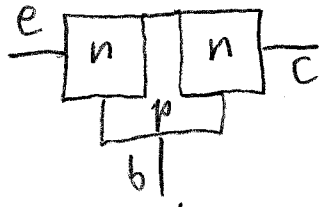
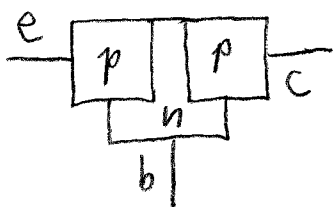
• WITH BASE DISCONNECTED, IT WORKS LIKE 2 OPPOSING DIODES, AND NO CURRENT CAN FLOW.



• A SMALL CURRENT INTO THE BASE SQUIRTS HOLES INTO THE DEPLETION REGION, ALLOWING CONDUCTION OF A LARGE CURRENT FROM c TO e.

THE WHOLE POINT OF A TRANSISTOR IS TO USE A SMALL, WEAK SIGNAL (AT THE BASE) TO CONTROL THE CONDUCTIVITY OF THE DEVICE. THIS PAVES THE WAY FOR SOLID STATE AMPLIFIERS, SWITCHING DEVICES, ETC.

## 2 KINDS OF BJT:



MEMORIZE THE CONVENTIONAL DIRECTIONS FOR  $i_c, i_b, i_e$ . THEY ARE ALL NORMALLY POSITIVE.

Q: ARE e AND c INTERCHANGEABLE?

A: NO, e IS MORE HEAVILY DOPED.

# TRANSISTOR MODEL ("LARGE SIGNAL MODEL")

KCL:  $i_e = i_c + i_b$

3 MODES OF OPERATION:

## I. ACTIVE MODE

ALMOST THE SAME

$0 < i_b \ll i_c < i_e$

$|V_b - V_e| = V_T \sim 0.6V$

$i_c = \beta i_b, \beta \gg 1$

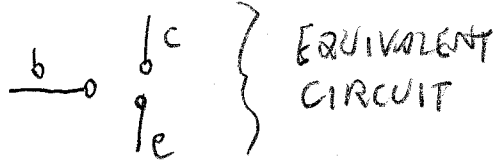
TYPICALLY,  $\beta \sim 50-300$ , BUT "POWER TRANSISTORS" CAN HAVE  $\beta \sim 20$ , AND "SUPER-BETA" TRANSISTORS  $\beta \sim 1500$ .

## II. CUTOFF MODE

IF  $\left\{ \begin{array}{l} \text{NPN: } V_b - V_e < V_T \\ \text{PNP: } V_e - V_b < V_T \end{array} \right\}$

THEN  $i_b = i_c = i_e = 0$

DEVICE IS TURNED OFF!

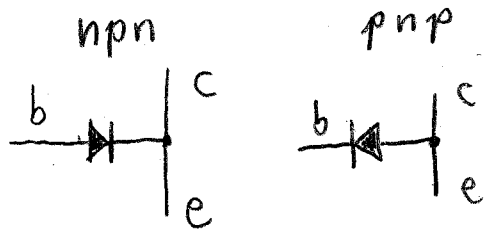


## III. SATURATED MODE

$i_b \neq 0, \text{ BUT } i_c < \beta i_b$

THIS HAPPENS WHEN THE EXTERNAL CIRCUITRY IS INCAPABLE OF PROVIDING ENOUGH CURRENT TO THE COLLECTOR. THE DEVICE TRIES ITS BEST BY MAXIMIZING CONDUCTANCE ACROSS THE COLLECTOR - EMITTER:

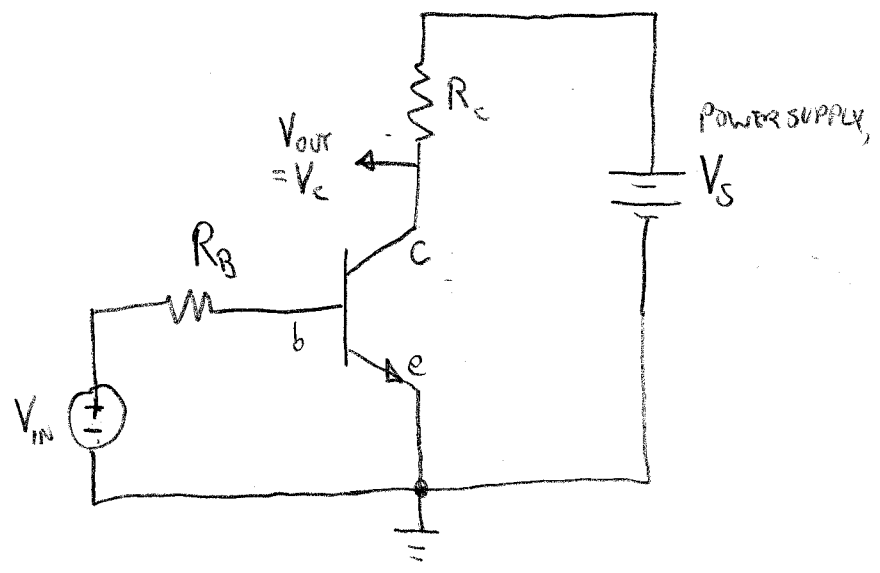
$V_c = V_e$



HOW DO I DETERMINE WHICH MODE A TRANSISTOR IS OPERATING IN? THE FOLLOWING PROCEDURE USUALLY WORKS:

- ① ASSUME ACTIVE MODE,  $i_c = \beta i_b$ .
- ② FIND  $i_b$ , CHECK FOR CUTOFF. IF SO,  $i_b = i_c = i_e = 0$ . STOP HERE.
- ③ FIND  $i_c$ , CHECK FOR SATURATION. IF SO,  $V_c = V_e$ .  
 $\Rightarrow$  RECALCULATE  $i_c$ .

EXAMPLE: COMMON-EMITTER AMPLIFIER (npn VERSION)



ASSUME ACTIVE MODE

$$i_b = \frac{V_{IN} - V_J}{R_B}$$

$$i_c = \beta i_b = \beta \left( \frac{V_{IN} - V_J}{R_B} \right)$$

$$V_{OUT} = V_S - i_c R_C = V_S - \beta \frac{R_C}{R_B} (V_{IN} - V_J)$$

$$= \underbrace{\left( V_S + \beta \frac{R_C}{R_B} V_J \right)}_{\text{CONSTANT OFFSET}} - \underbrace{\beta \frac{R_C}{R_B} V_{IN}}_{\text{AMPLIFIED SIGNAL}}$$

$$\text{GAIN} = -\beta \frac{R_C}{R_B}$$

CUTOFF: IF  $V_{IN} < V_J$ ,  $i_b = 0 \Rightarrow i_c = 0 \Rightarrow V_{OUT} = V_S = \text{const.}$   
 SO CUTOFF AT  $V_{OUT} = V_S$  WHEN  $V_{IN} < V_J$

SATURATION: MAX  $i_c$  CORRESPONDS TO  $V_C = V_{OUT} = 0$ .

IF THE ACTIVE MODE SOLN LEADS TO  $V_{OUT} < 0$ , THEN WE SATURATE:

$$V_{OUT} < 0 \iff \beta \frac{R_C}{R_B} V_{IN} > V_S + \beta \frac{R_C}{R_B} V_J$$

$\therefore$  WE SATURATE ( $V_{OUT} \rightarrow 0$ ) WHEN  $V_{IN} > V_J + \frac{R_B}{\beta R_C} V_S$